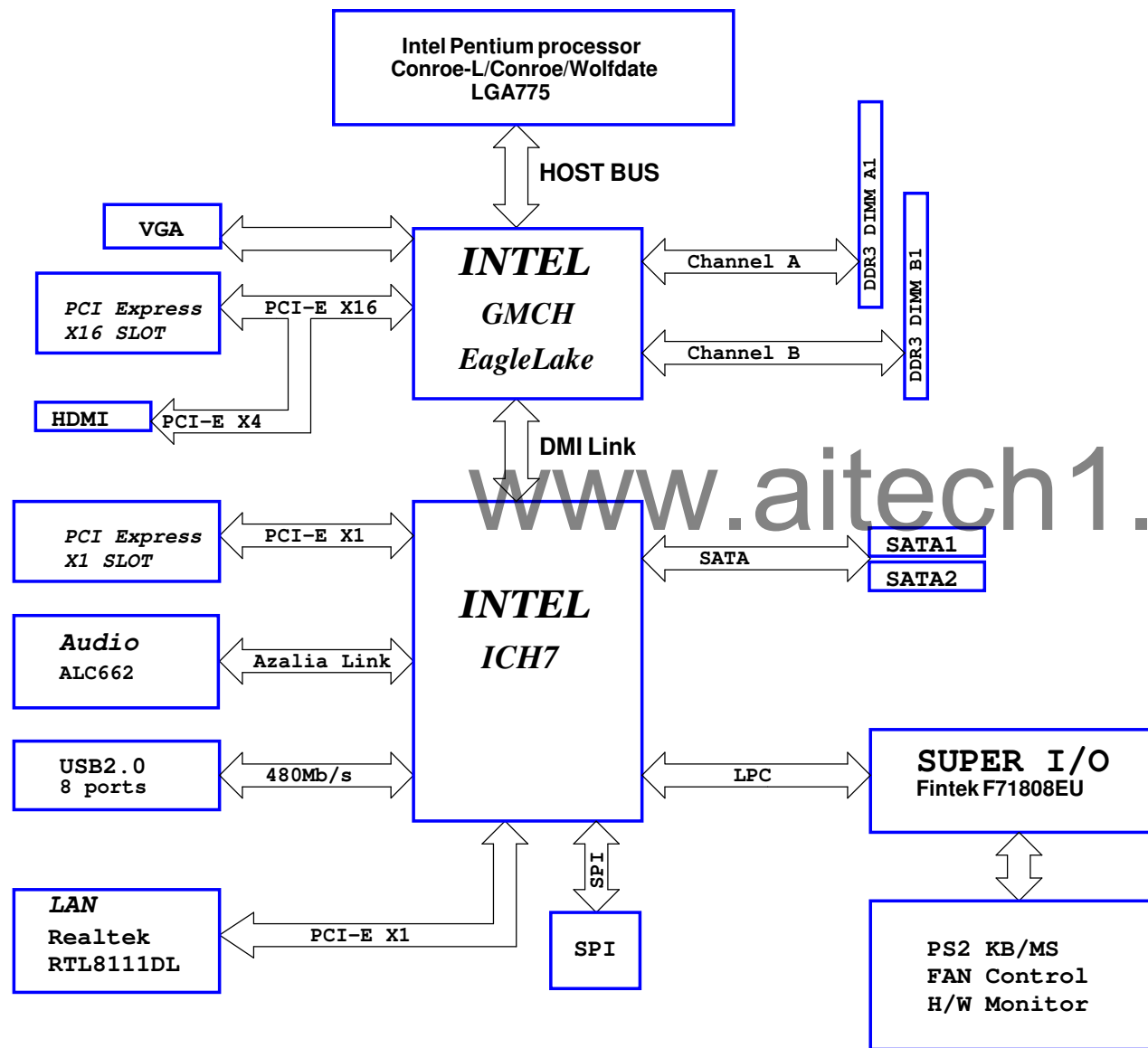


IPX41-D3

Revision:1.02

53	33.+5V_DUAL	2
54	54.+3P3V_PCIE&+3P3V_LAN	
55		
56		

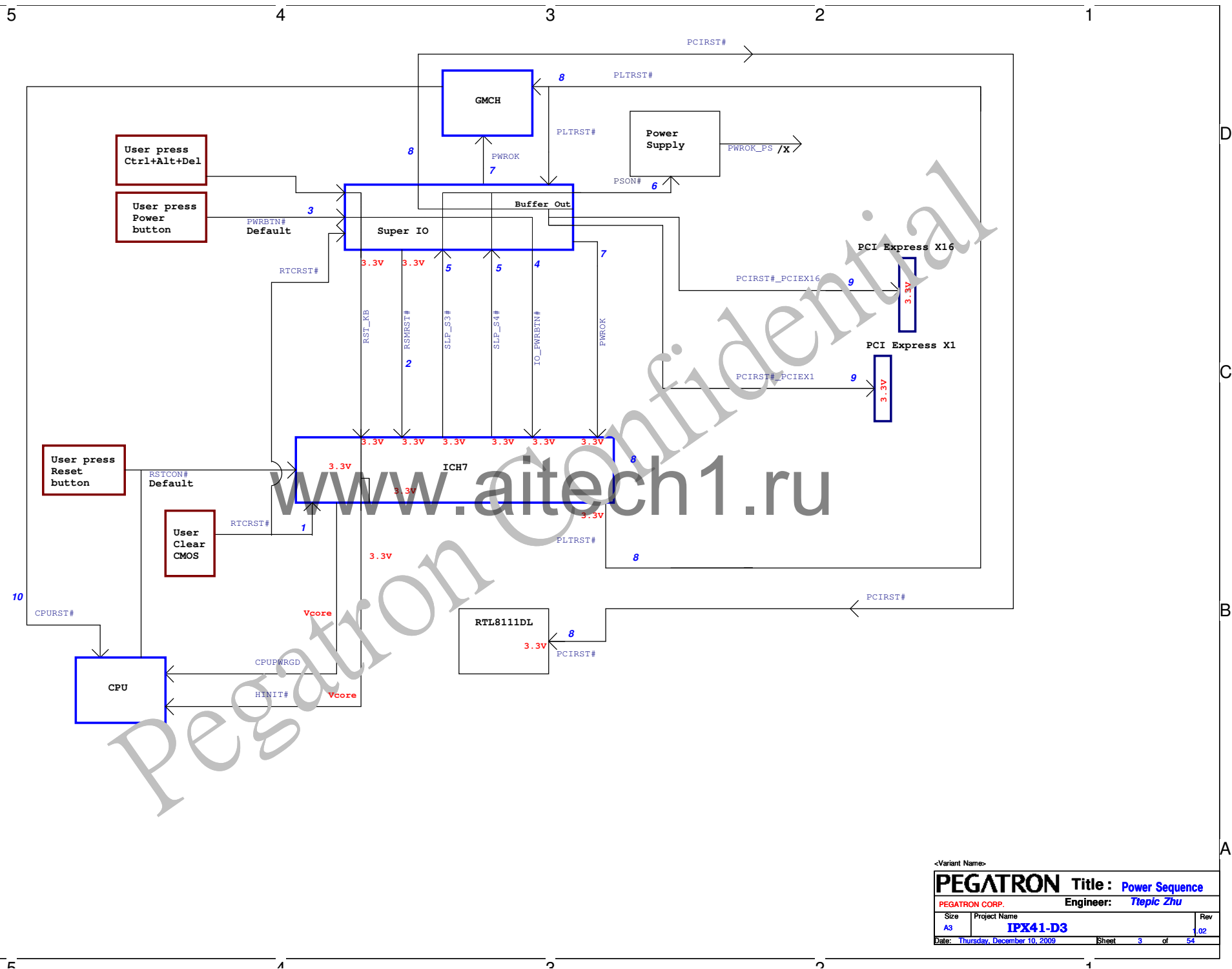
01	01.Block Diagram	1
02	02.ECN CONTROL TABLE	
03	03.Power Sequence	
04	04.Power Flow	
05	05.Clock Distribution	
06	06.CLOCK	
07	07.PROCESSOR LGA775 1 - 3	
08	08.PROCESSOR LGA775 2 - 3	
09	09.PROCESSOR LGA775 3 - 3	
10	10.INTEL EAGLELAKE 1 - 7	
11	11.INTEL EAGLELAKE 2 - 7	
12	12.INTEL EAGLELAKE 3 - 7	
13	13.INTEL EAGLELAKE 4 - 7	
14	14.INTEL EAGLELAKE 5 - 7	
15	15.INTEL EAGLELAKE 6 - 7	
16	16.INTEL EAGLELAKE 7 - 7	
17	17.DDR3 CHANNEL A	
18	18.DDR3 CHANNEL B	
19	19.DDR3 TERMINATION A&B	
20	20.INTEL ICH7 1 - 4	
21	21.INTEL ICH7 2 - 4	
22	22.INTEL ICH7 3 - 4	
23	23.INTEL ICH7 4 - 4	
24	24.PCI EXPRESS X1 SLOT	
25	25.PCI EXPRESS X16 SLOT	
26	26.INTEGRATED VGA PORT	
27	27.DVI/HDMI CONTROL	
28	28.DVI&HDMI / PCIE MUX	
29	29.DVI&HDMI LEVEL SHIFTER	
30	30.DVI&HDMI CONNECTOR	
31	31.USB CON.	
32	32.USB HEADER CONNECTOR	
33	33.SATA CONNECTOR FOR CPC	
34	34.Realtek RTL8111DL	
35	35.RJ-45+USB CONNECTOR	
36	36.REALTEK ALC662 AZALIA CODEC	
37	37.REAR AUDIO CONNECTOR	
38	38.EMI CAP	
39	39.SUPER I/O - F71808EU	
40	40.PS2 KB &MS CONNECTOR FOR CPC	
41	41.FAN CIRCUIT	
42	42.FRONT PANEL CIRCUIT FOR CPC	
43	43.SPI SERIAL FLASH LPC DEGUG	
44	44.RTC / CMOS / SPKR/SCREW HOLE	
45	45.ATX POWER 24P CONNECTOR	
46	46.VCORE CONTROLLER	
47	47.VCORE DRIVER1	
48	48.VCORE DRIVER2	
49	49.+1P1V_CORE	
50	50.+1P1V_FSB VTT	
51	51.VTT_DDR&3P3VSB SWITCHING&1P5	
52	52.+1P5V_DUAL	

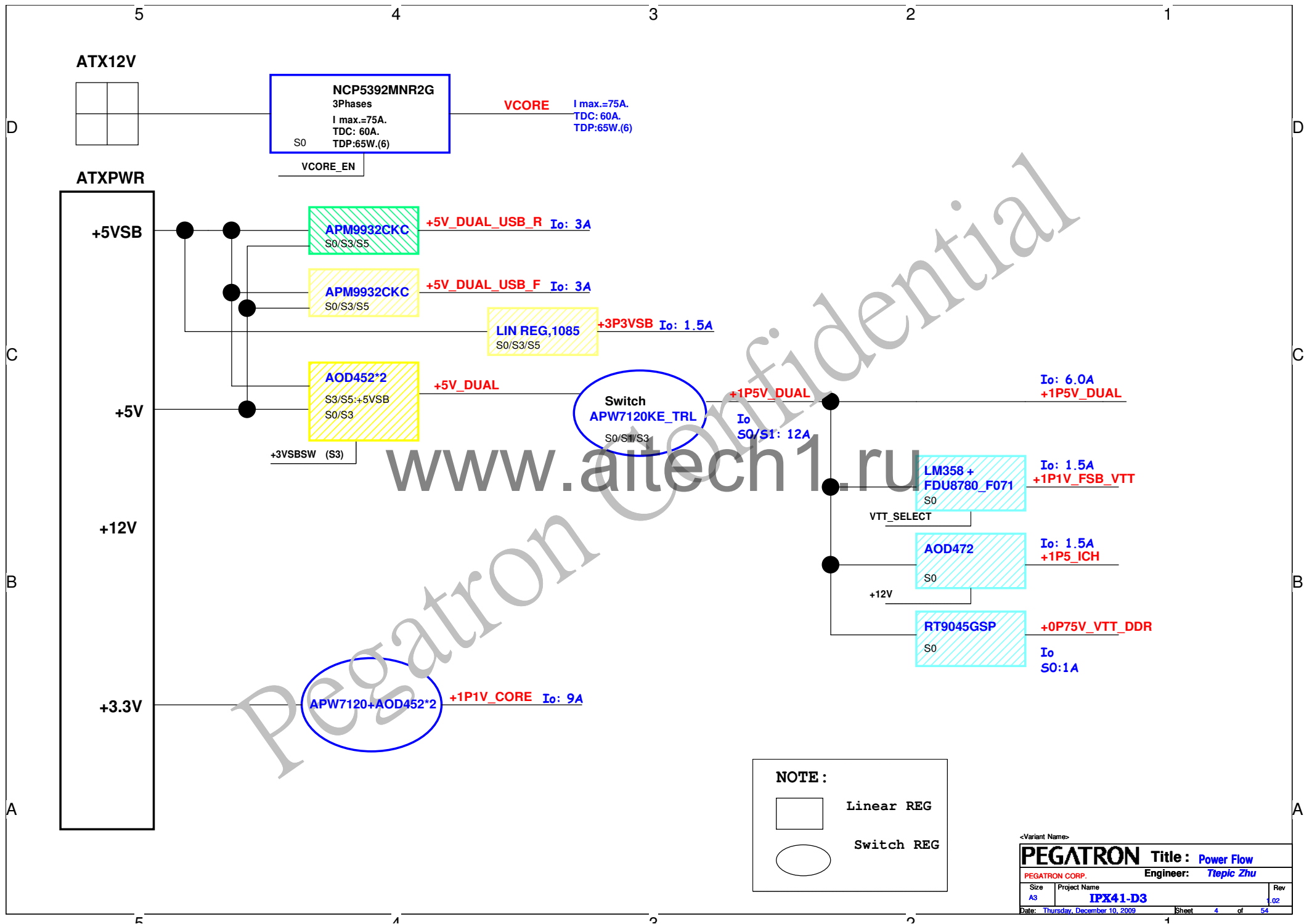


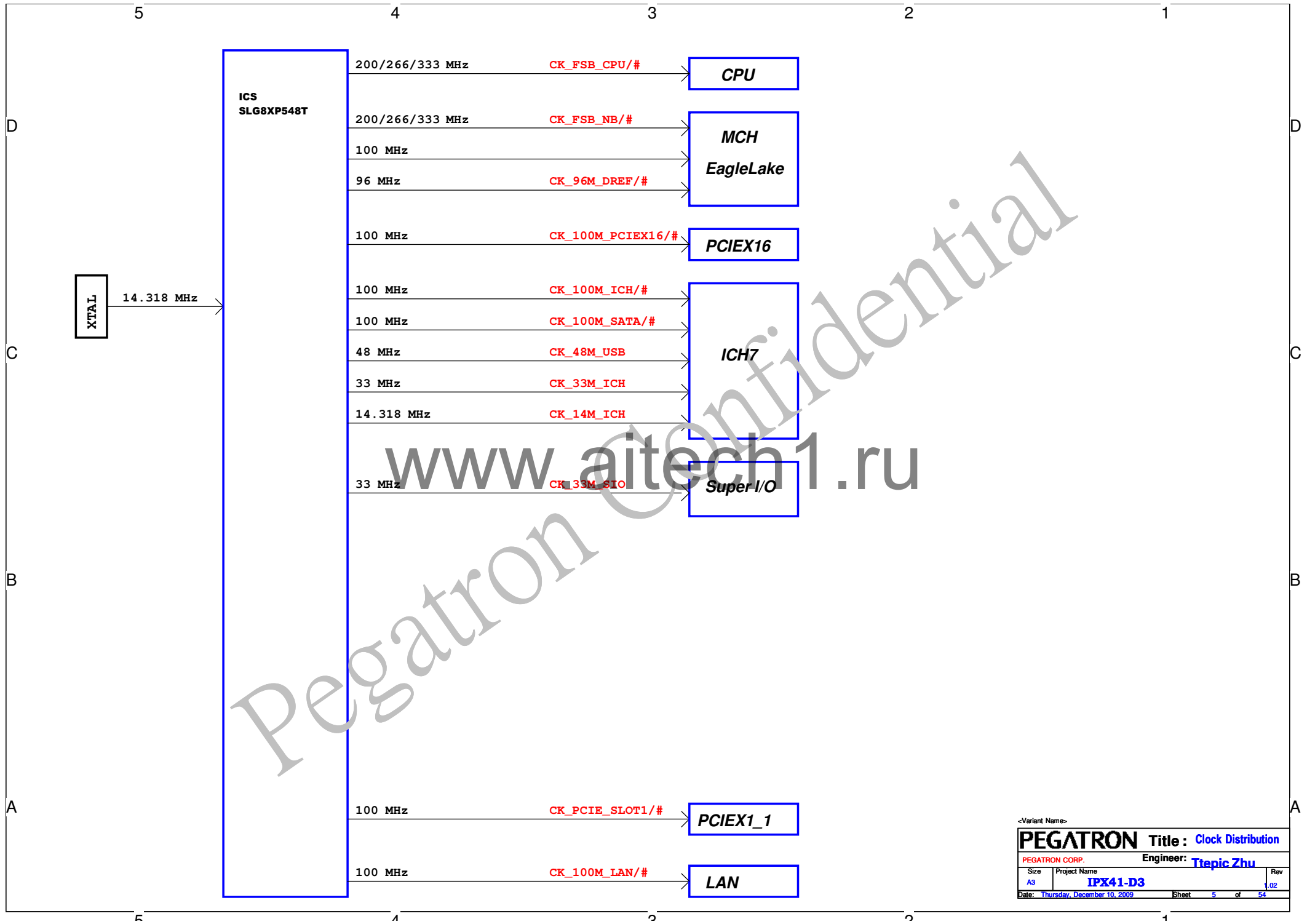
ECN Control Table

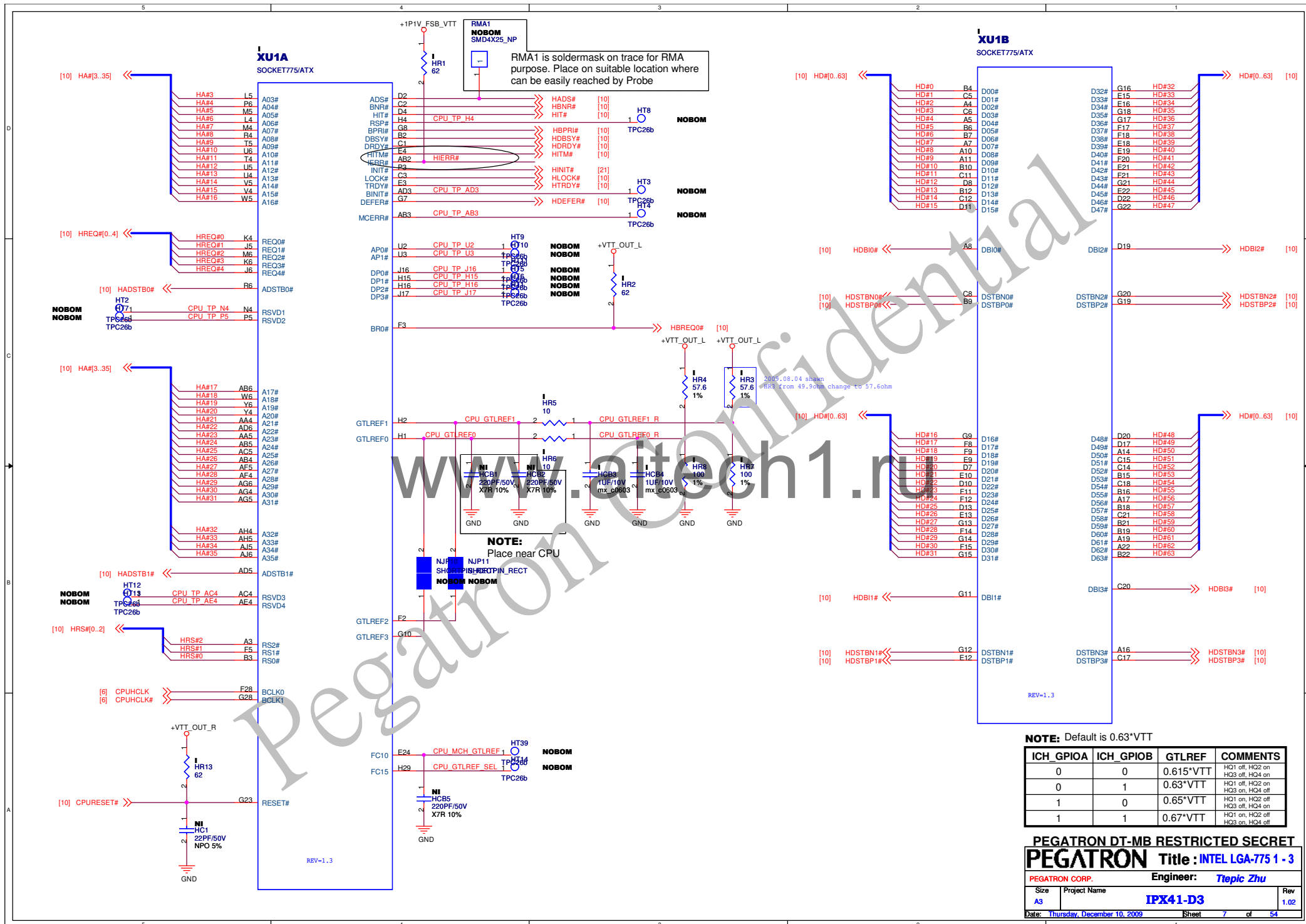
ECN No.	DATE	Subject	Schematics Revision	BOM Part Number	PCBA Revision	PCB Revision

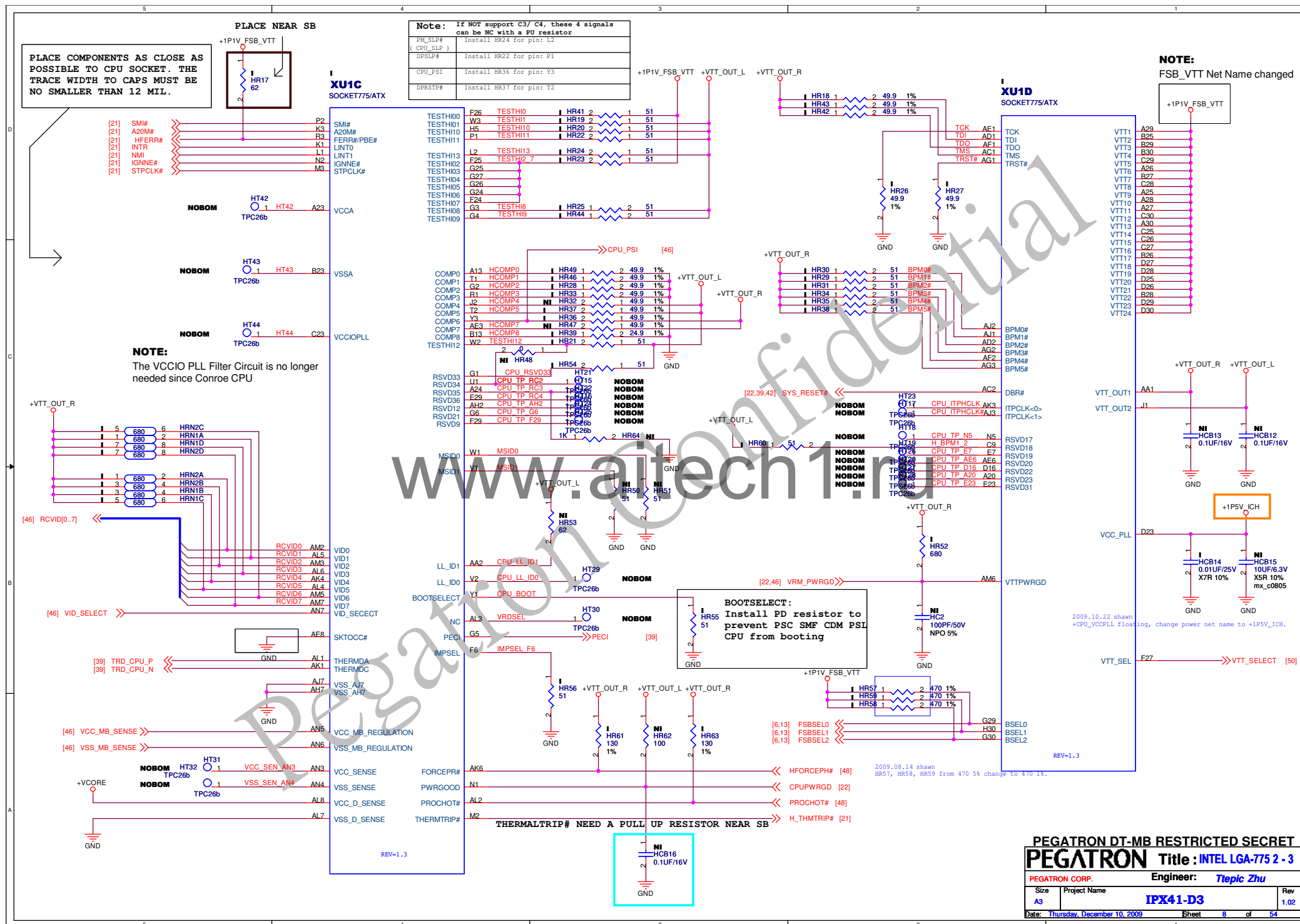
www.aitech1.ru

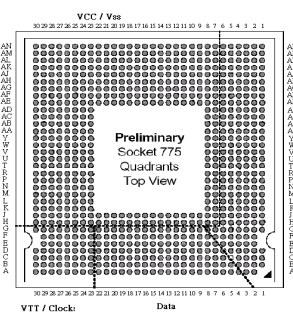
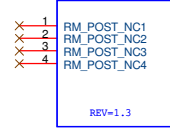
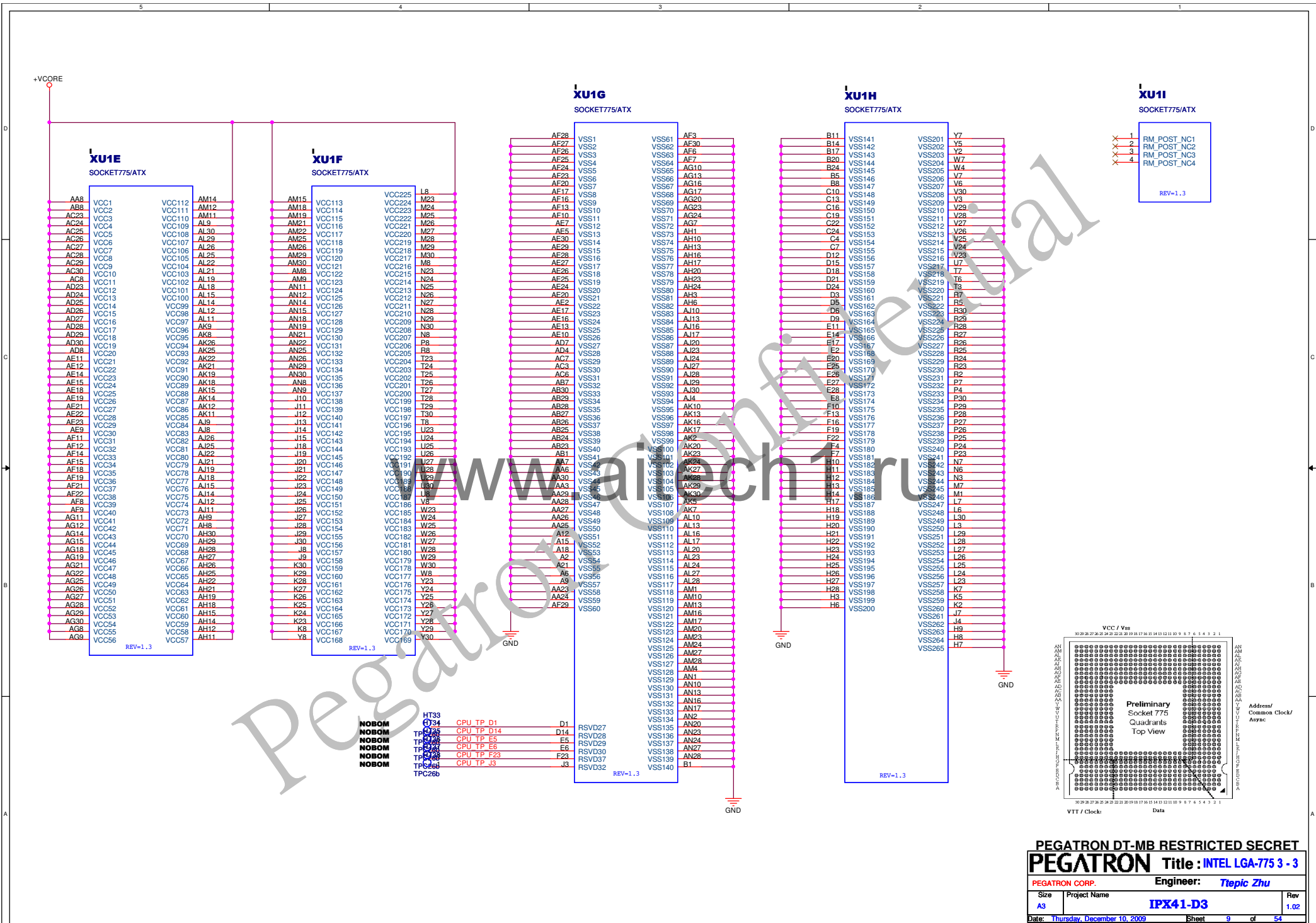




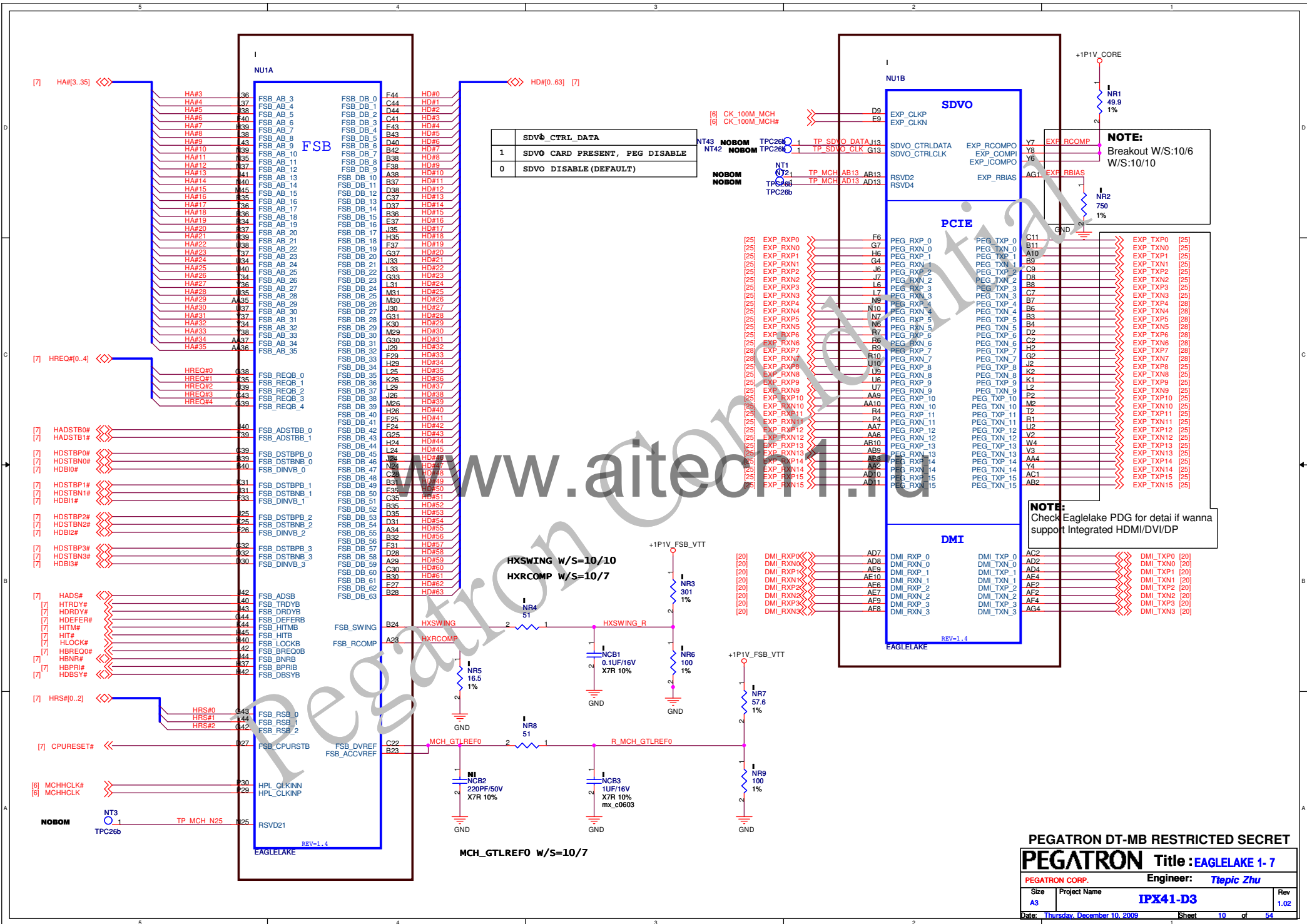








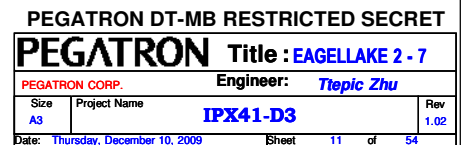
NOBOM	HT33	CPU TP D1	D1	RSVD27
NOBOM	TPC26	CPU TP D14	D14	RSVD28
NOBOM	TPC27	CPU TP E5	E5	RSVD29
NOBOM	TPC28	CPU TP E6	E6	RSVD30
NOBOM	TPC29	CPU TP F23	F23	RSVD31
NOBOM	TPC30	CPU TP J3	J3	RSVD32
NOBOM	TPC26b			

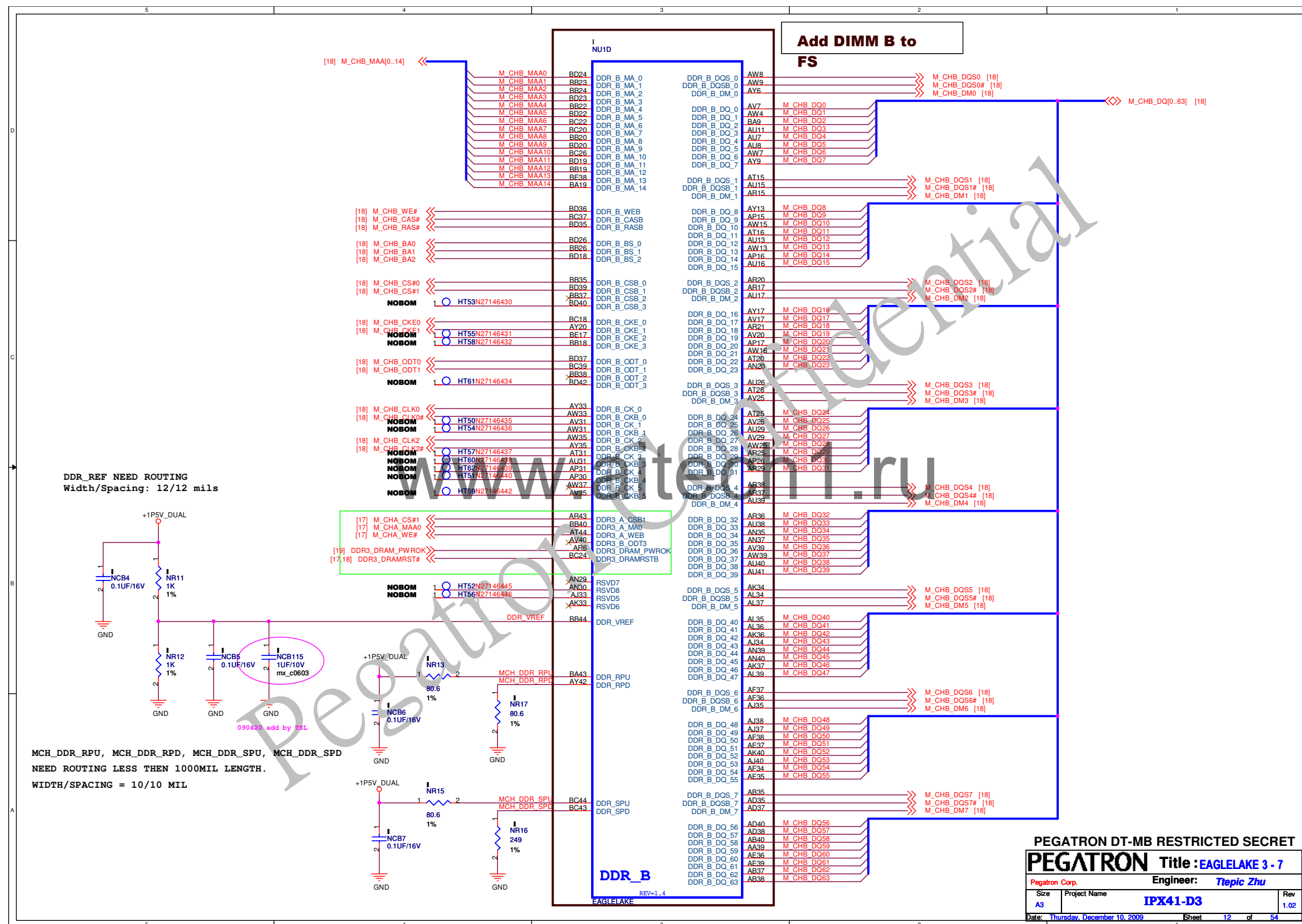


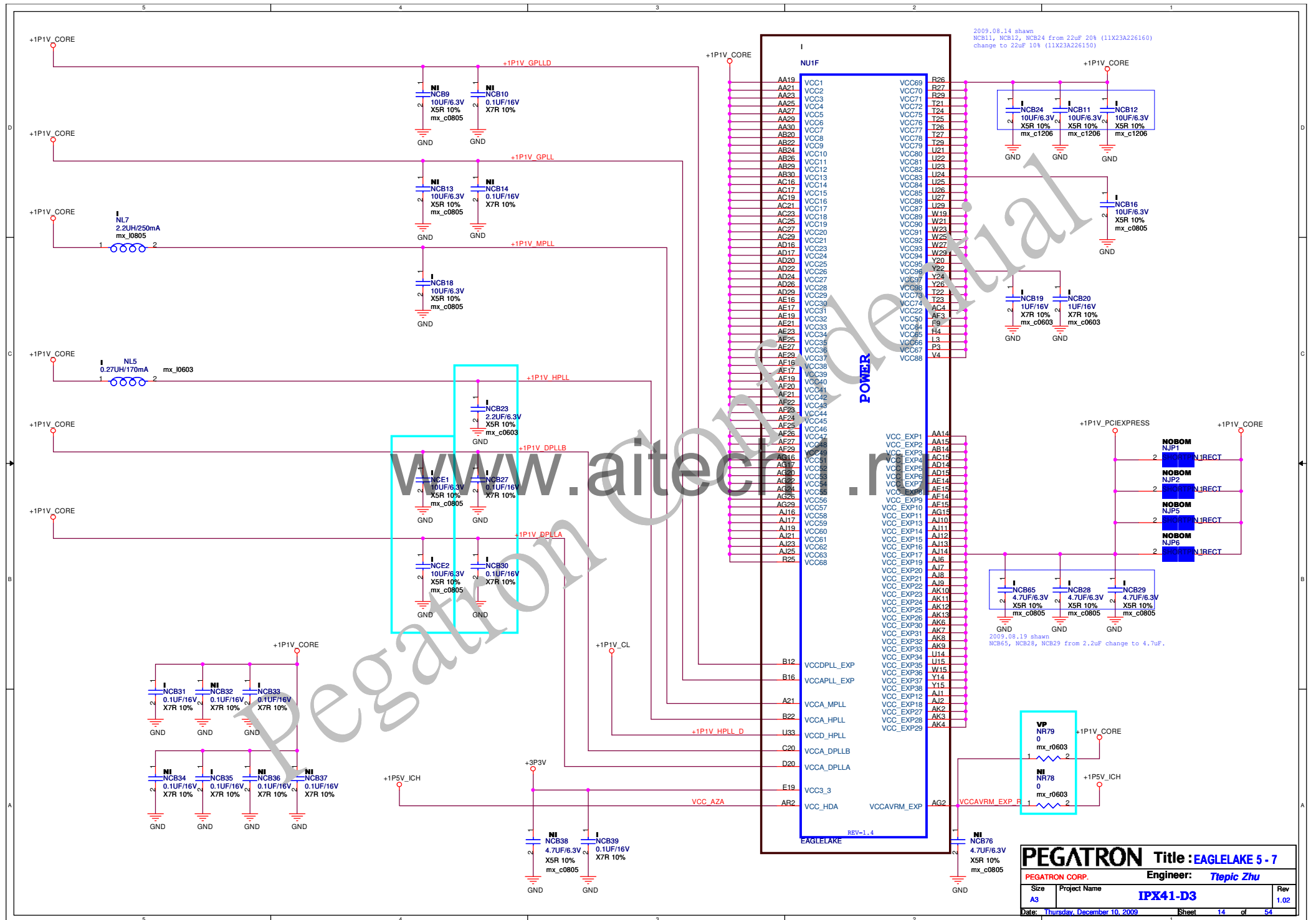
SDVO_CTRL_DATA			
1	SDVO CARD PRESENT, PEG DISABLE		
0	SDVO DISABLE (DEFAULT)		

NOTE:
Breakout W/S:10/6
W/S:10/10

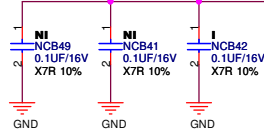
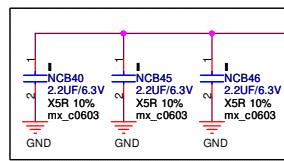
NOTE:
Check Eaglelake PDG for detai if wanna support Integrated HDMI/DVI/DP



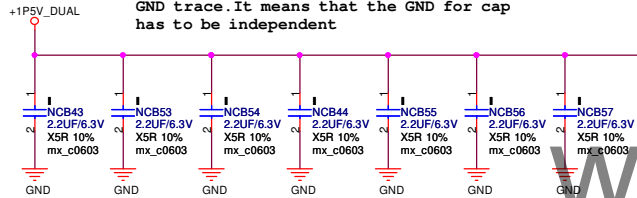




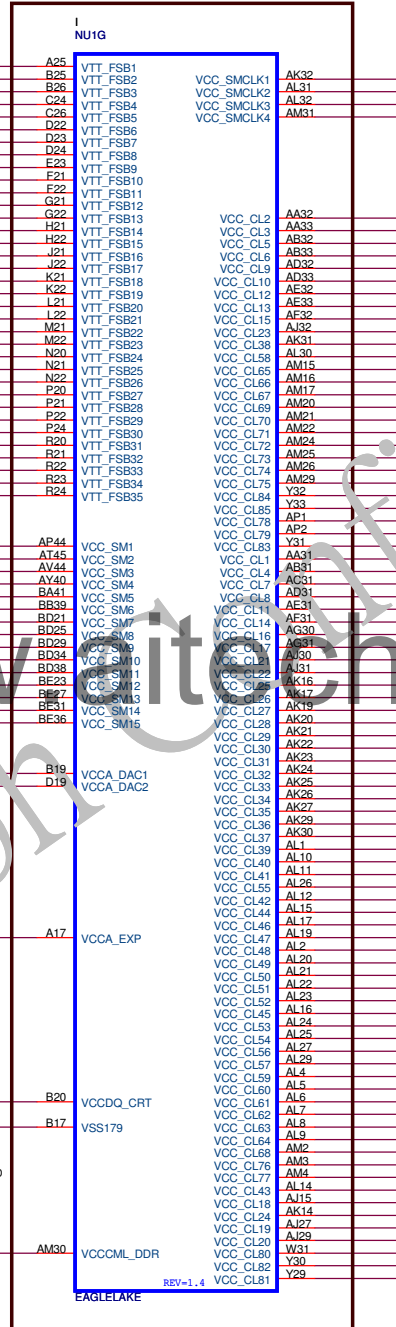
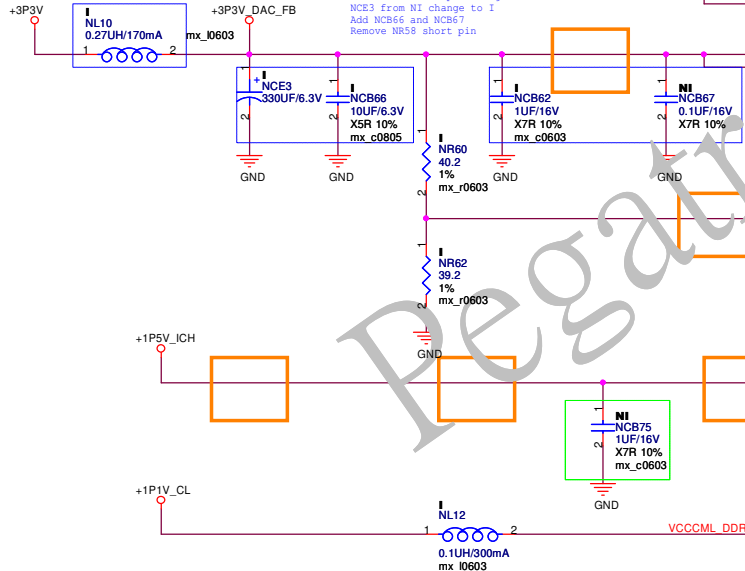
Place near GMCH



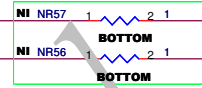
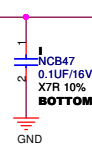
Place a via in between cap and GMCH on GND trace. It means that the GND for cap has to be independent



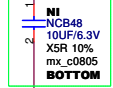
2009.09.29 shawn
NL10 from short-pin change to 0.27uF
NCE3 from NI change to I
Add NCB66 and NCB67
Remove NR58 short pin



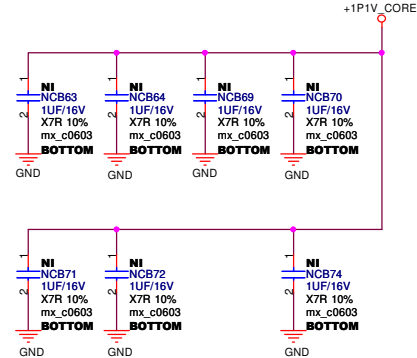
VCCCK_DDR



+1P5V_DUAL



BACKSIDE CAPS FOR SPECIFIC +1P1V_CORE GMCH

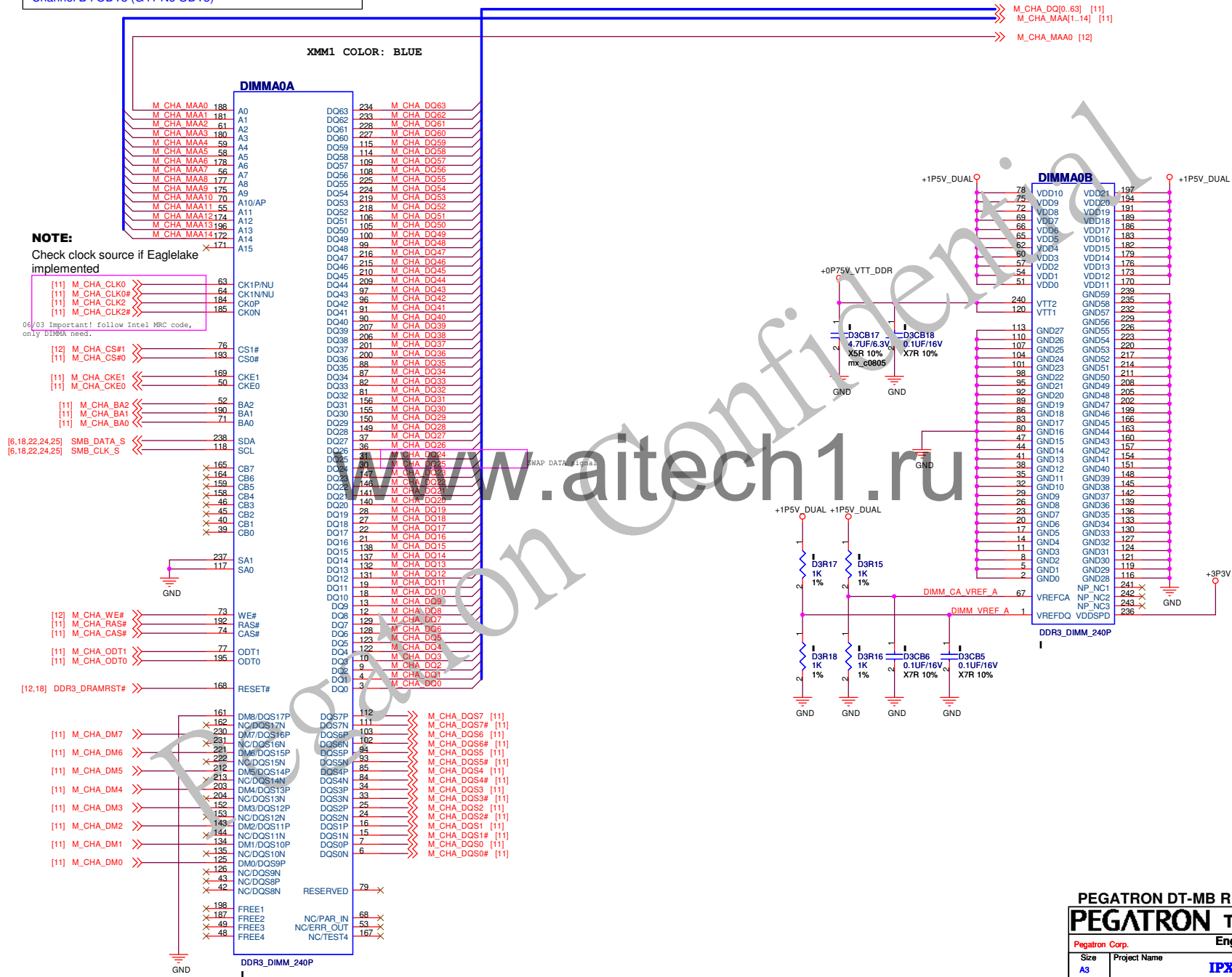


PEGATRON DT-MB RESTRICTED SECRET

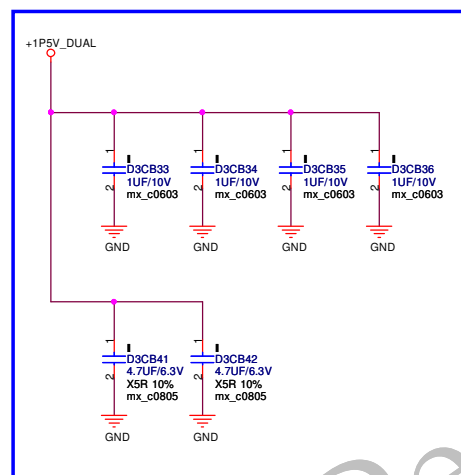
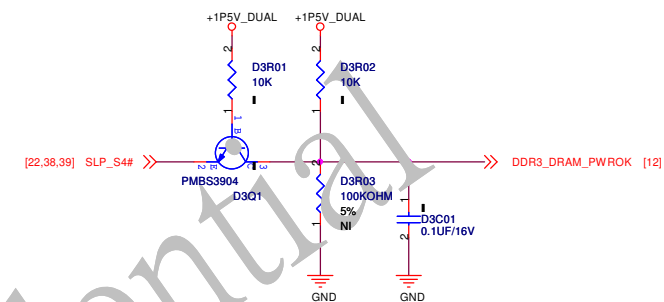
PEGATRON Title: EAGLELAKE 6 - 7

PEGATRON CORP.	Engineer: Topic Zhu
Size A3	Project Name IPX41-D3
Date: Thursday, December 10, 2009	Sheet 15 of 54

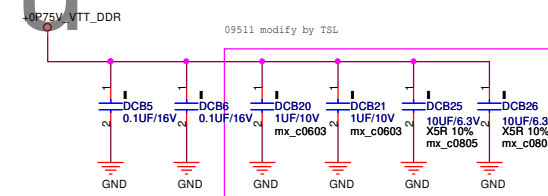
NOTE:
Below 4 signals are different connection in Eaglelake platform
Channel A : CS1/WE/MA0
Channel B : ODT3 (G41 No ODT3)



PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title: DDR3 DIMMA	
Pegatron Corp.		Engineer: <i>Tepic Zhu</i>	
Size A3	Project Name IPX41-D3		Rev 1.02
Date: Thursday, December 10, 2009		Sheet 17 of 54	



09511 modify by TSL



09511 modify by TSL

PEGATRON DT-MB RESTRICTED SECRET

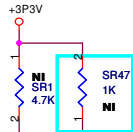
PEGATRON Title : DDR3 Termination A&B

Engineer: Ttepic Zhu

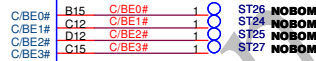
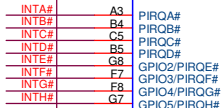
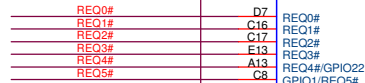
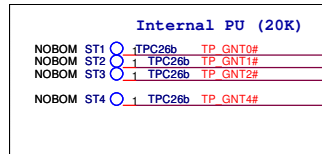
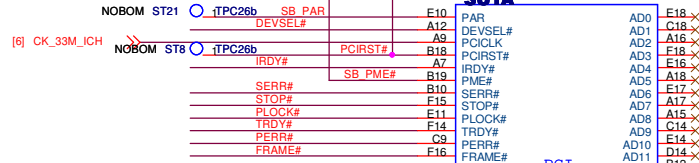
Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 19 of 54

PME# internal pull up to +3VSB (20k)

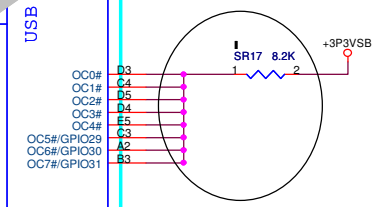
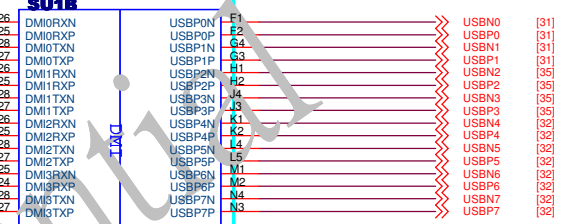
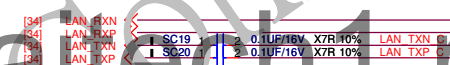
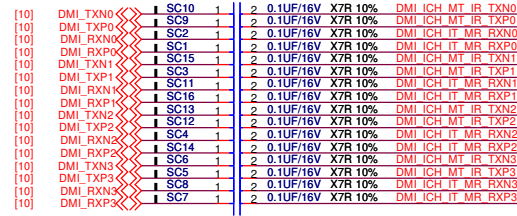
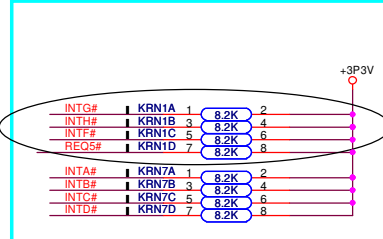
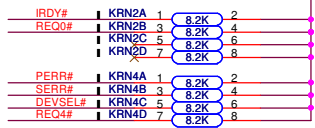
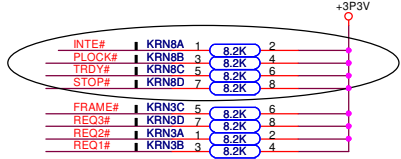


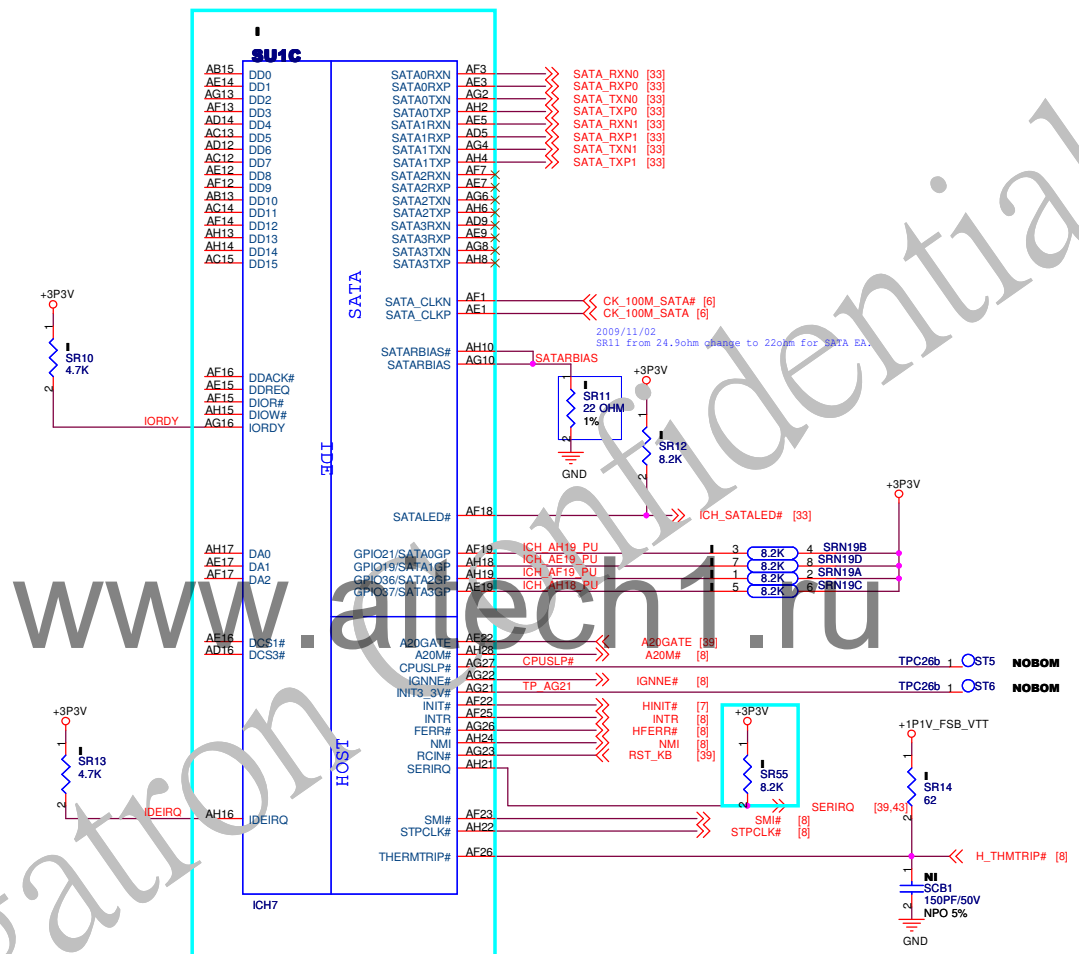
Place capacity near ICH7 by
CDI / IBL Doc # 367652 Eaglelake PDG 1.5

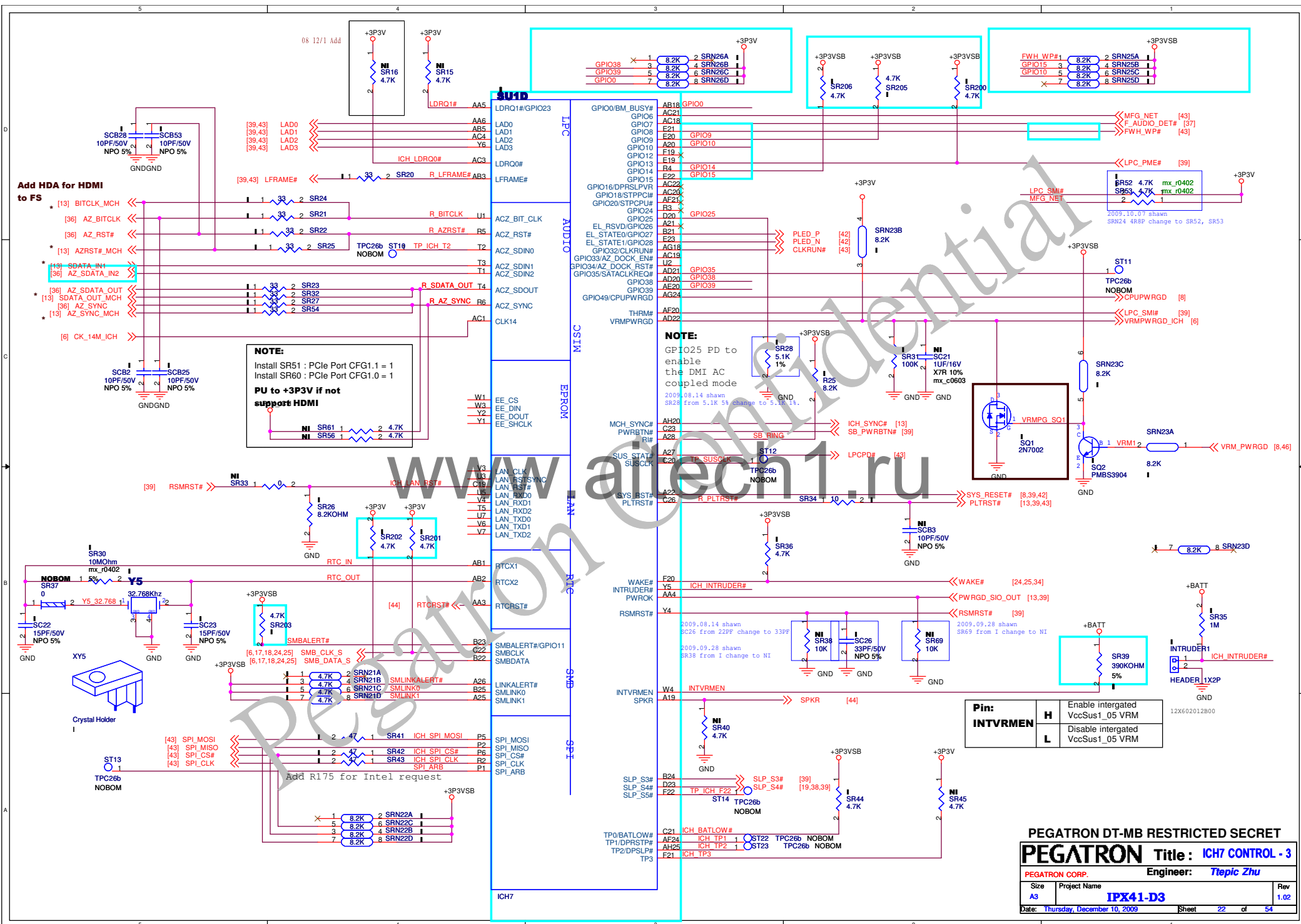


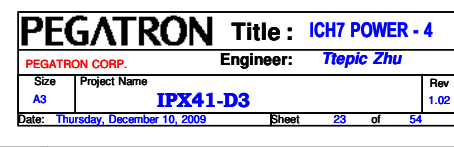
GNT5, REQ5 NEED BIOS PROGRAM

SR9	Option	Action
NI	FWH ROM	Default
1Kohm	SPI ROM	Select

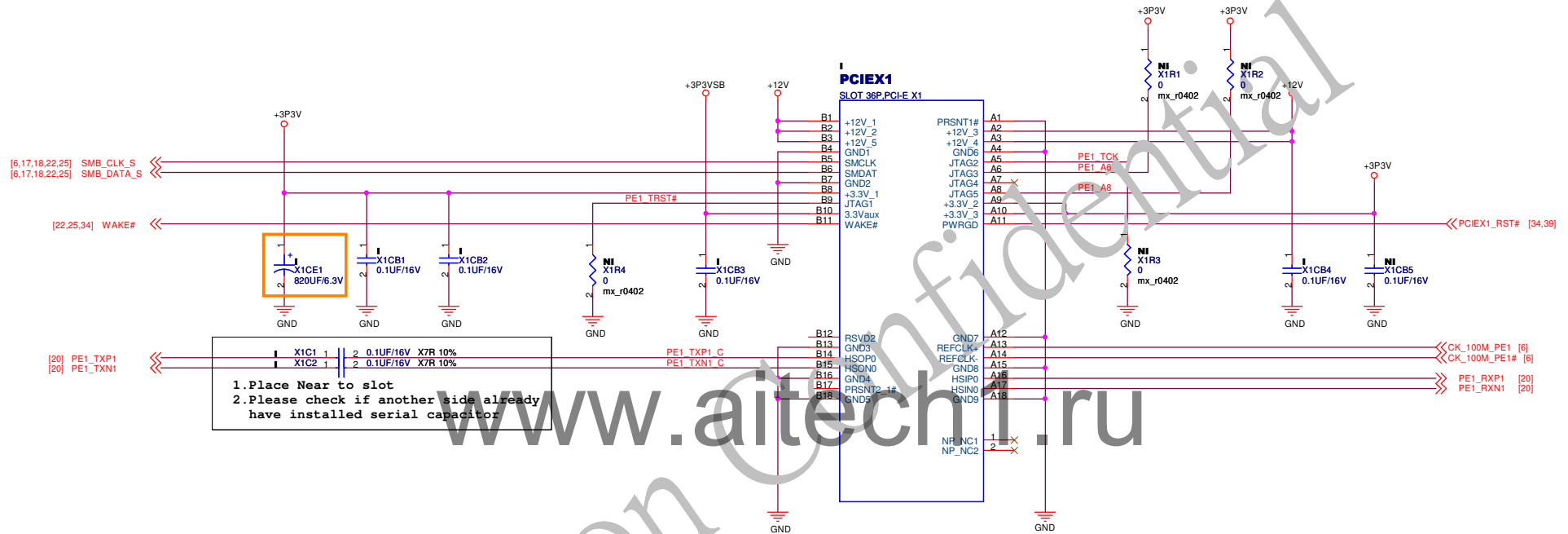




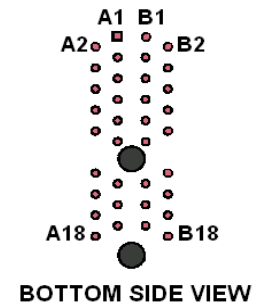
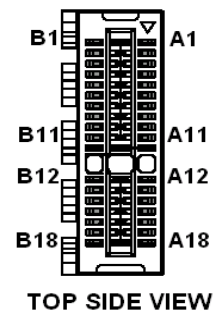




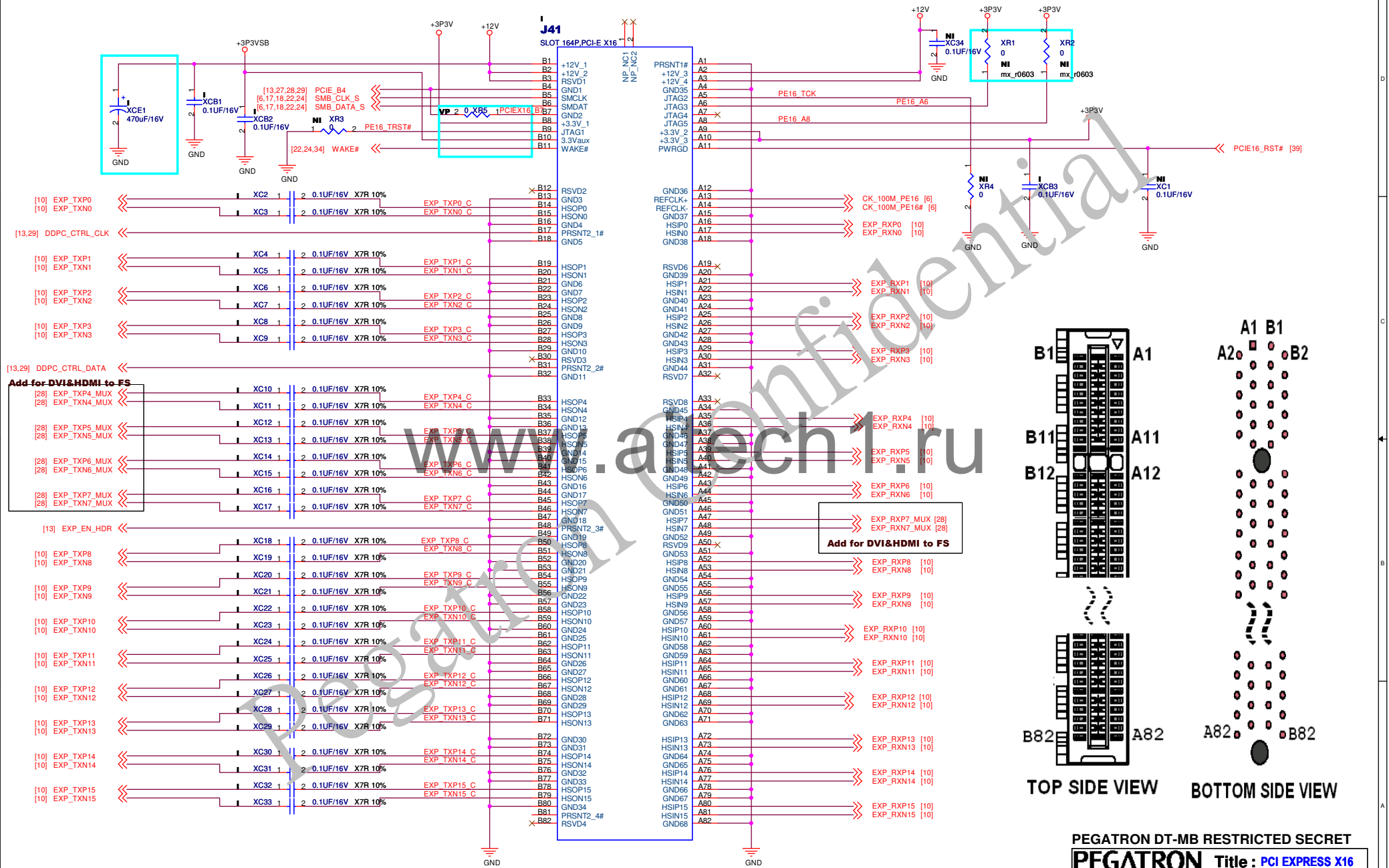
PCI Express x1 SLOT



1. Place Near to slot
2. Please check if another side already have installed serial capacitor



PCI EXPRESS X16 Graphics Card Slot



PEGATRON DT-MB RESTRICTED SECRET

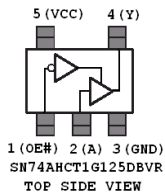
PFGATRON Title : PCI EXPRESS X16

PEGATRON CORP. **Engineer:** *Tiepic Zhu*

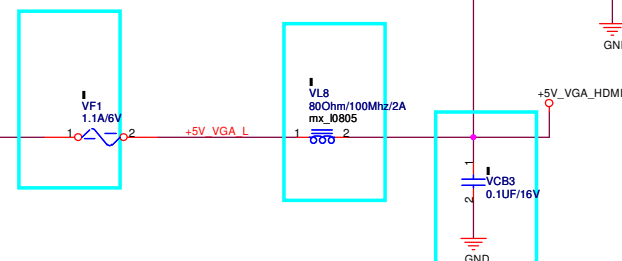
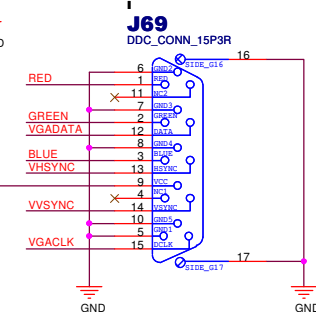
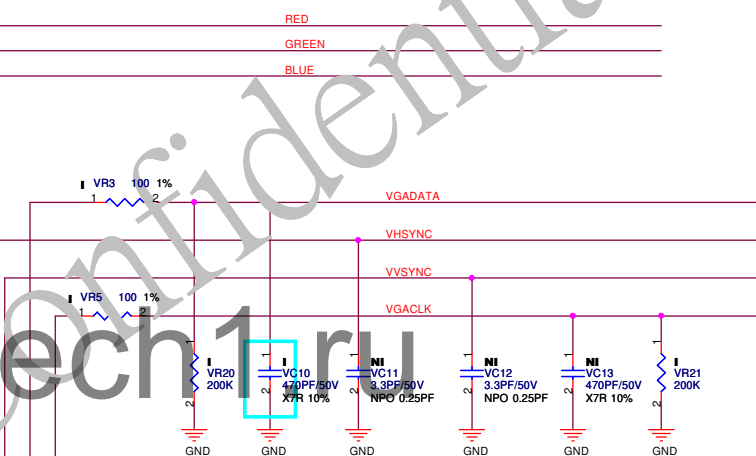
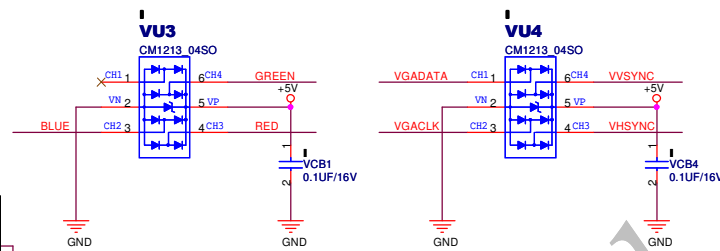
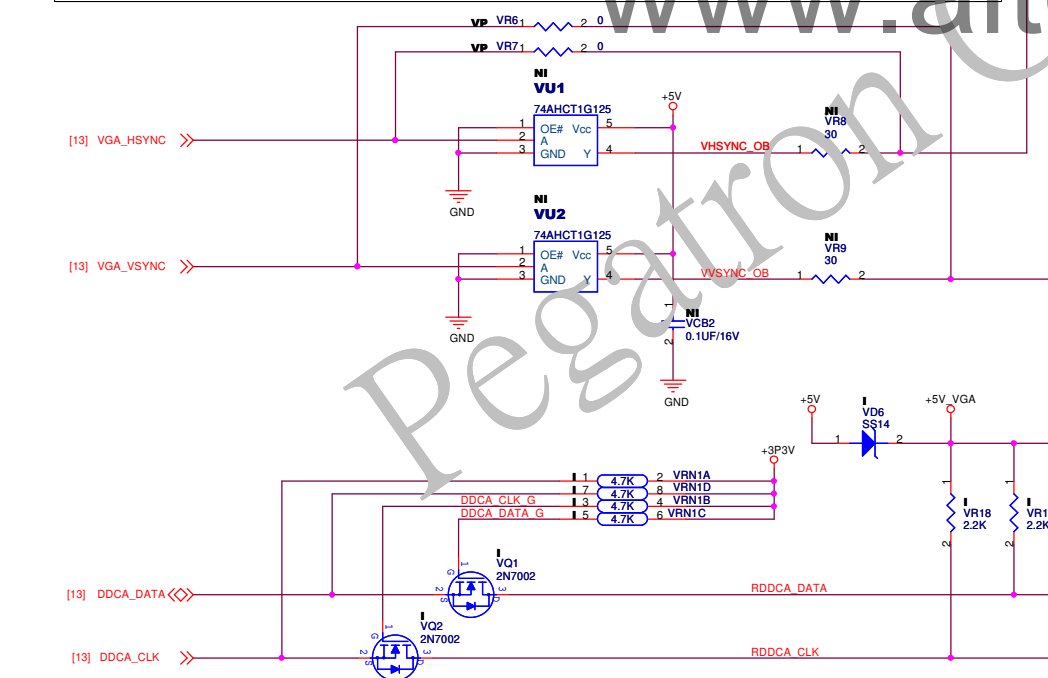
Size	Project Name	Rev
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A3	IPX41-D3	1.02
Date: Thursday, December 10, 2009	Sheet 25 of 54	

[illegible]

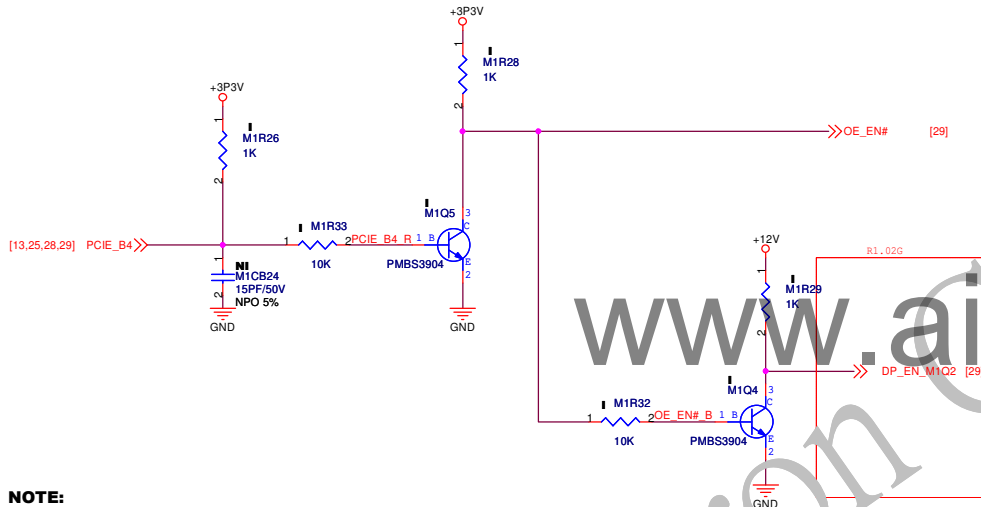


NOTE:
Place there VGA filter components
within 500 mils of the VGA connector



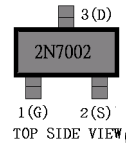
Add HDMI CONTROL to FS

Digital Port Switch Control Logic



NOTE:

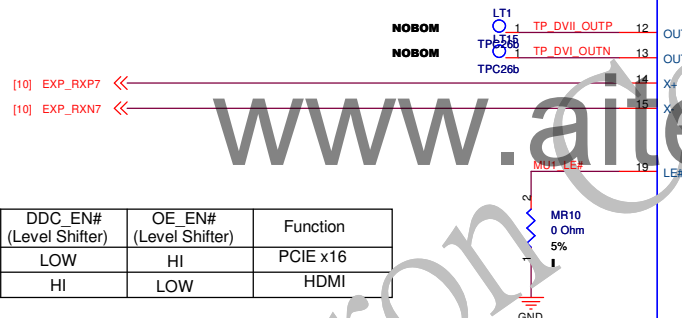
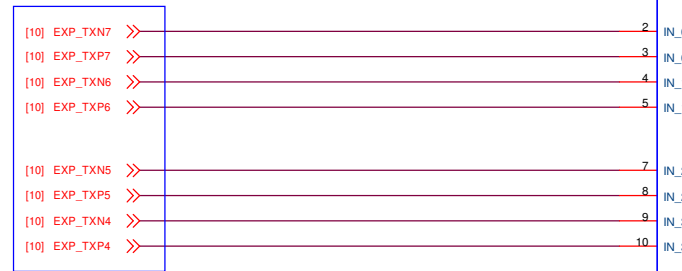
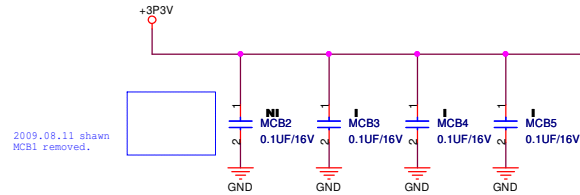
PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	HDMI



PEGATRON DT-MB RESTRICTED SECRET

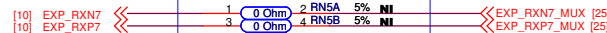
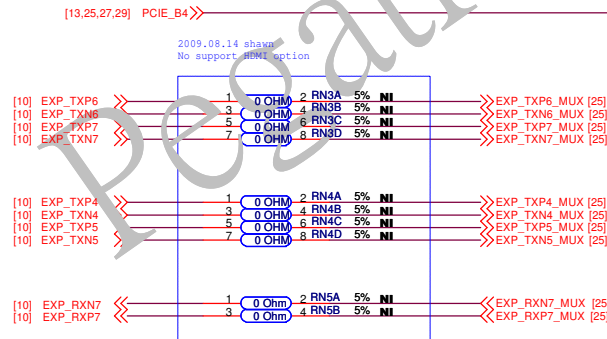
PEGATRON		Title : HDMI CONTROL	
PEGATRON CORP.		Engineer: Teping Zhu	
Size A3	Project Name IPX41-D3	Rev 1.02	
Date: Thursday, December 10, 2009		Sheet	27 of 54

Add HDMI / PCIE MUX to FS

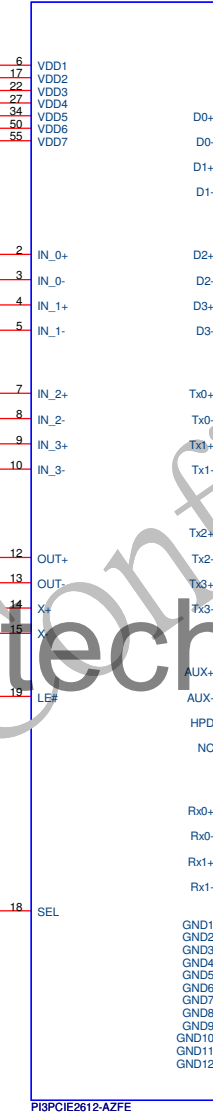


NOTE:

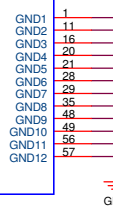
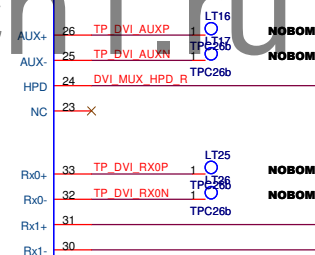
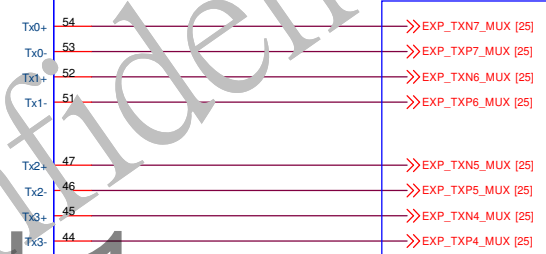
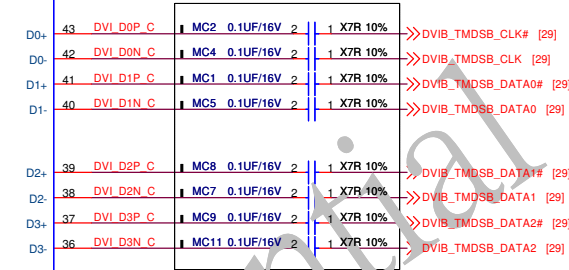
PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	HDMI



MU1

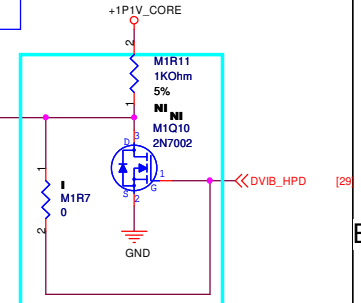


NOTE: Place near Level Shifter



NOTE: HPD status

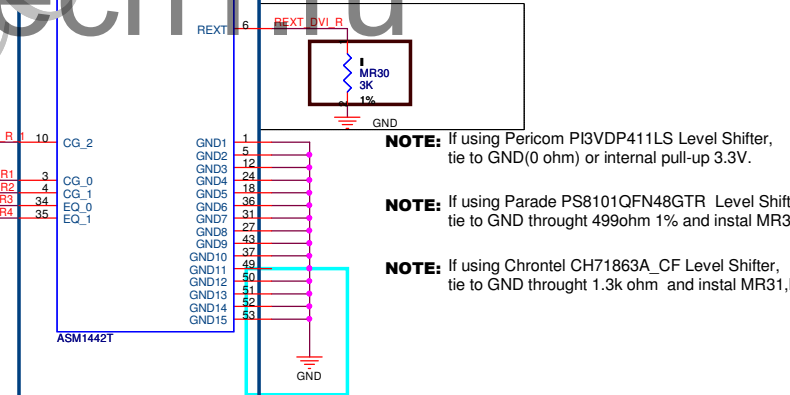
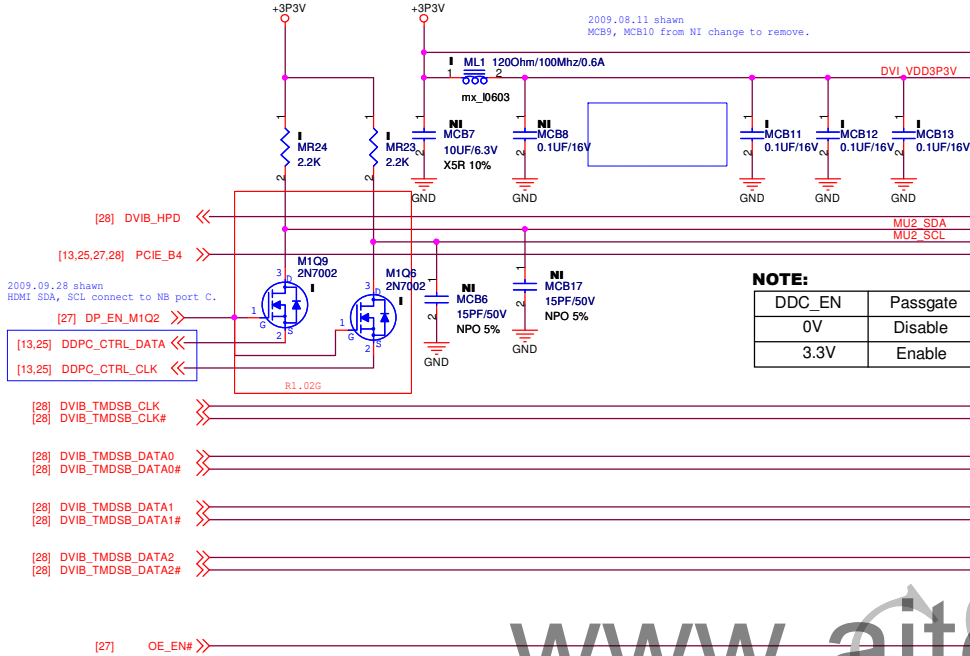
HI	DVI plugged
LOW	DVI unplugged



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : HDMI / PCIE MUX	
PEGATRON CORP.		Engineer: Ttepic Zhu	
Size A3	Project Name IPX41-D3	Rev 1.02	
Date: Thursday, December 10, 2009		Sheet 28 of 54	

Add HDMI LEVEL SHIFTER to FS



NOTE: Pericom PI3VDP411LS

Pin 3, 4, 6, 10, 34, and 35 are internal 100K ohm pull-up

OC_3 (Pin10)	OC_2 (Pin6)	OC_1 (Pin4)	OC_0 (Pin3)	Vswing (mV)	Pre/Deemphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

NOTE: Pericom PI3VDP411LS

EQ0 (Pin34)	EQ1 (Pin35)	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

NOTE:

OE*	IN_D Termination	OUT_D Outputs
1	Hi-Z	Hi-Z
0	50ohm	Active

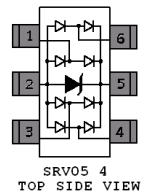
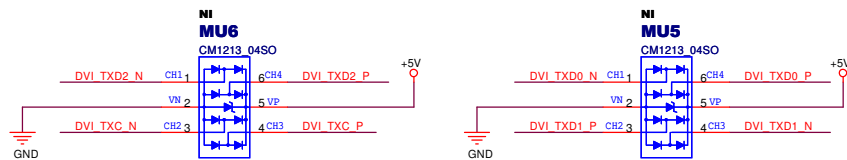
NOTE: If using Pericom PI3VDP411LS Level Shifter, tie to GND(0 ohm) or internal pull-up 3.3V.

NOTE: If using Parade PS8101QFN48GTR Level Shifter, tie to GND through 499ohm 1% and instal MR33.

NOTE: If using Chrontel CH71863A_CF Level Shifter, tie to GND through 1.3k ohm and instal MR31,MR32.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : HDMI LEVEL SHIFTER	
PEGATRON CORP.		Engineer: Ttepic Zhu	
Size A3	Project Name IPX41-D3	Rev 1.02	
Date: Thursday, December 10, 2009		Sheet 29 of 54	

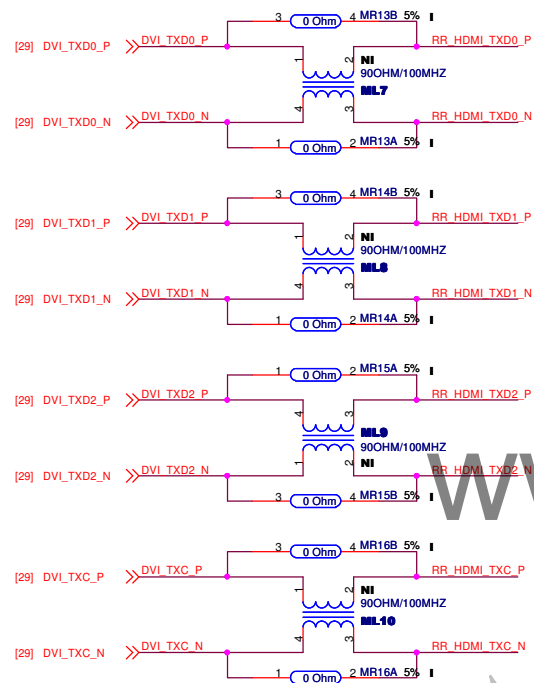


NOTE:

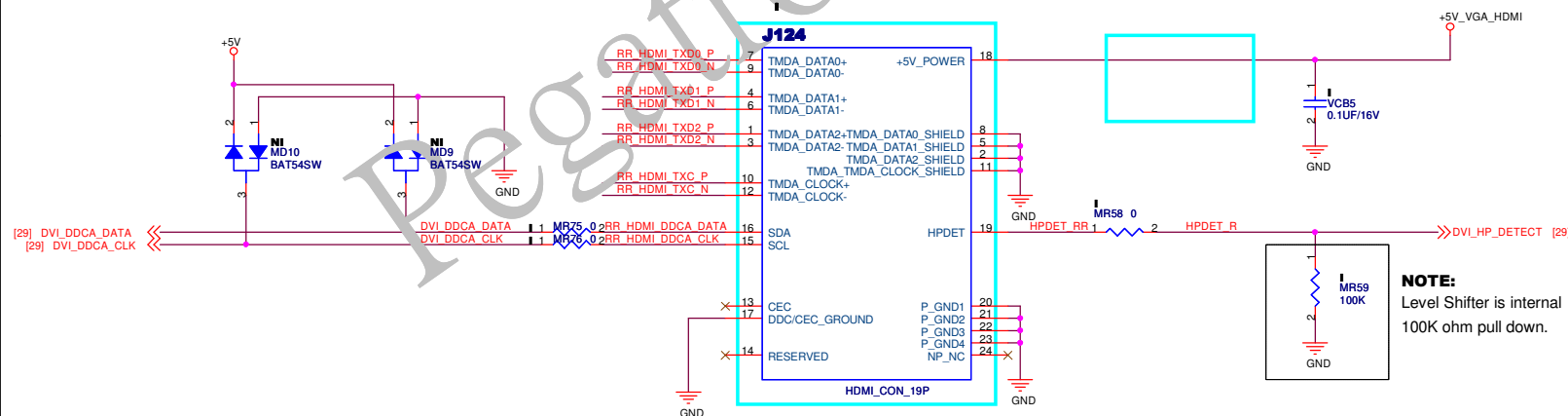
Level Shifter is internal 100K ohm pull down.

NOTE: HPDET status

High	Plugged
Low	Unplugged



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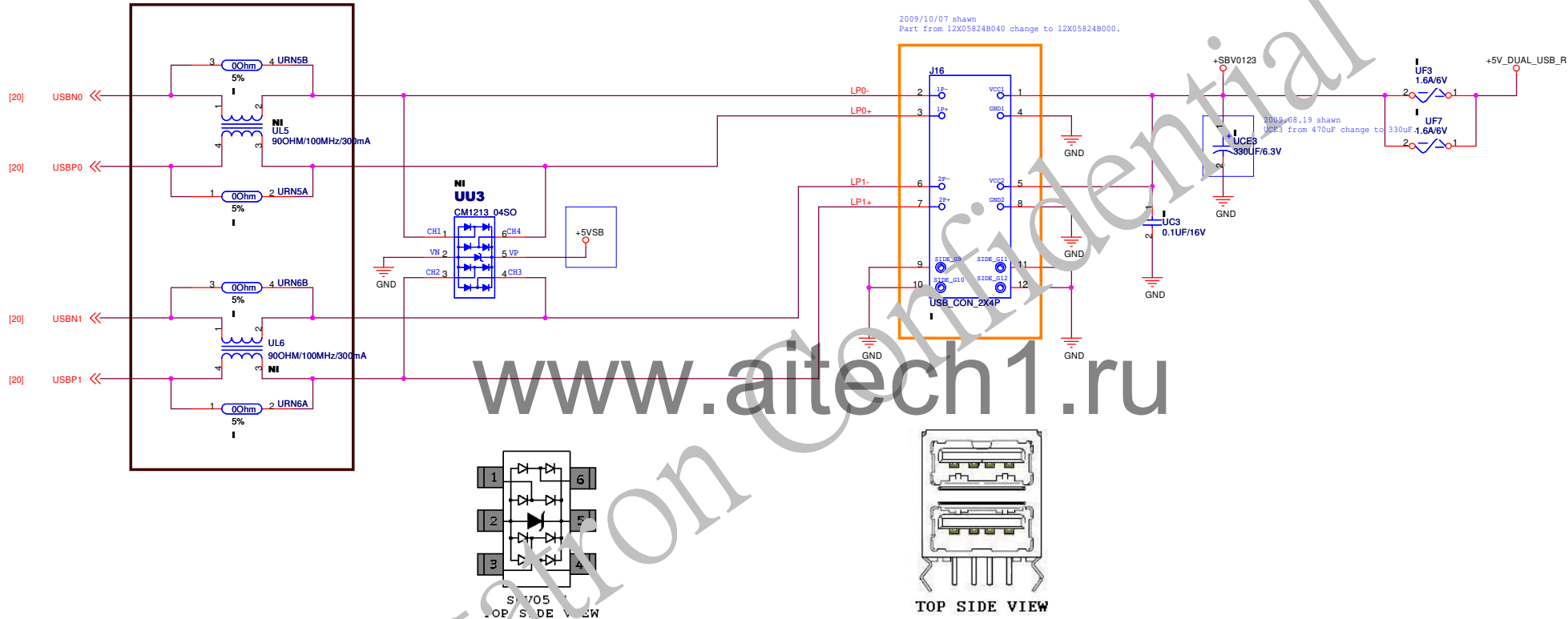


NOTE:

Level Shifter is internal 100K ohm pull down.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : HDMI PORT	
PEGATRON CORP.		Engineer: Tepic Zhu	
Size	Project Name	IPX41-D3	Rev
A3			1.02
Date: Thursday, December 10, 2009		Sheet	30 of 54

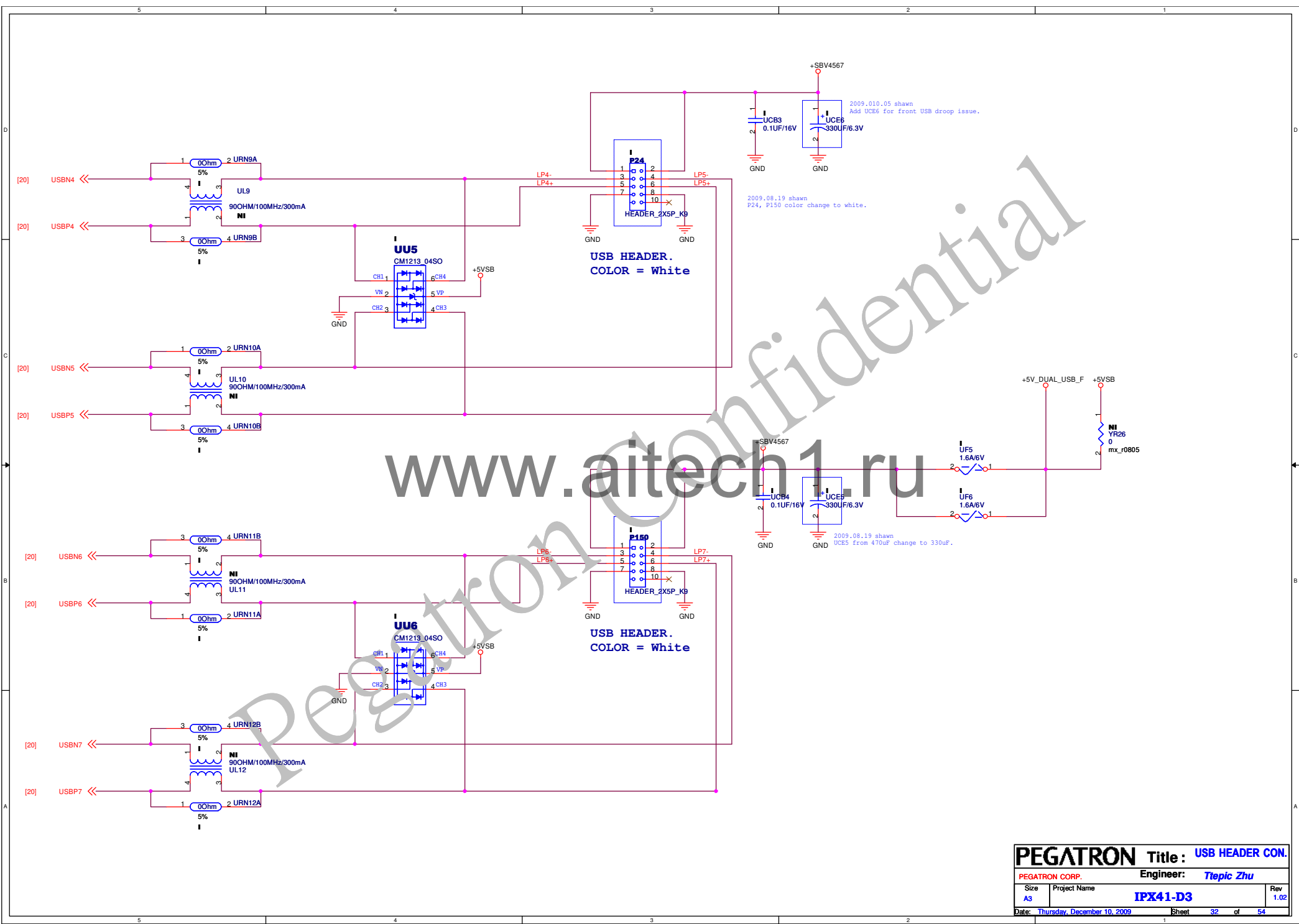


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title: **DOUBLE USB CON.**

Pegatron Corp.		Engineer: Tiepic Zhu	
Size A3	Project Name IPX41-D3	Rev 1.02	
Date: Thursday, December 10, 2009	Sheet 31	of 54	

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The schematic diagram illustrates the electrical connections for the HD LED and SATA interface on the AITECH1 module. It includes the following components and connections:

- HD LED:** A blue LED labeled **TD2 BAT54AW** is connected to the **HD_LED# [42]** signal. The anode (pin 1) is connected to the signal line, and the cathode (pin 2) is connected to **GND**. Pin 3 is also shown.
- SATA CON.:** A connector labeled **SATA CON. COLOR = Orange** is shown with pins 1 through 7.
 - Pins 1, 2, 3, and 4 are connected to **P_GND1**.
 - Pins 5, 6, and 7 are connected to **P_GND2**.
 - The connector is also labeled **SATA_CON_7P**.
- SATA Signals:** The SATA connector is connected to four SATA data lines:
 - SATA_TXP1_C** (Pin 1)
 - SATA_TXN1_C** (Pin 2)
 - SATA_RXN1_C** (Pin 3)
 - SATA_RXP1_C** (Pin 4)
- Termination:** The SATA data lines are terminated at the other end by four termination components labeled **TC21**, **TC22**, **TC23**, and **TC24**.
- Capacitors:** Each termination component (TC21-TC24) is connected to a capacitor labeled **2 0.01UF/25V X7R 10%**.
- Grounding:** The capacitors are connected to **GND**.



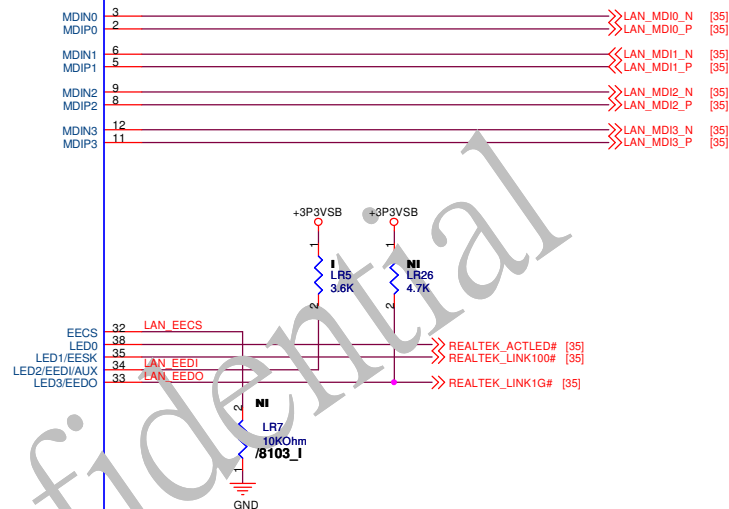
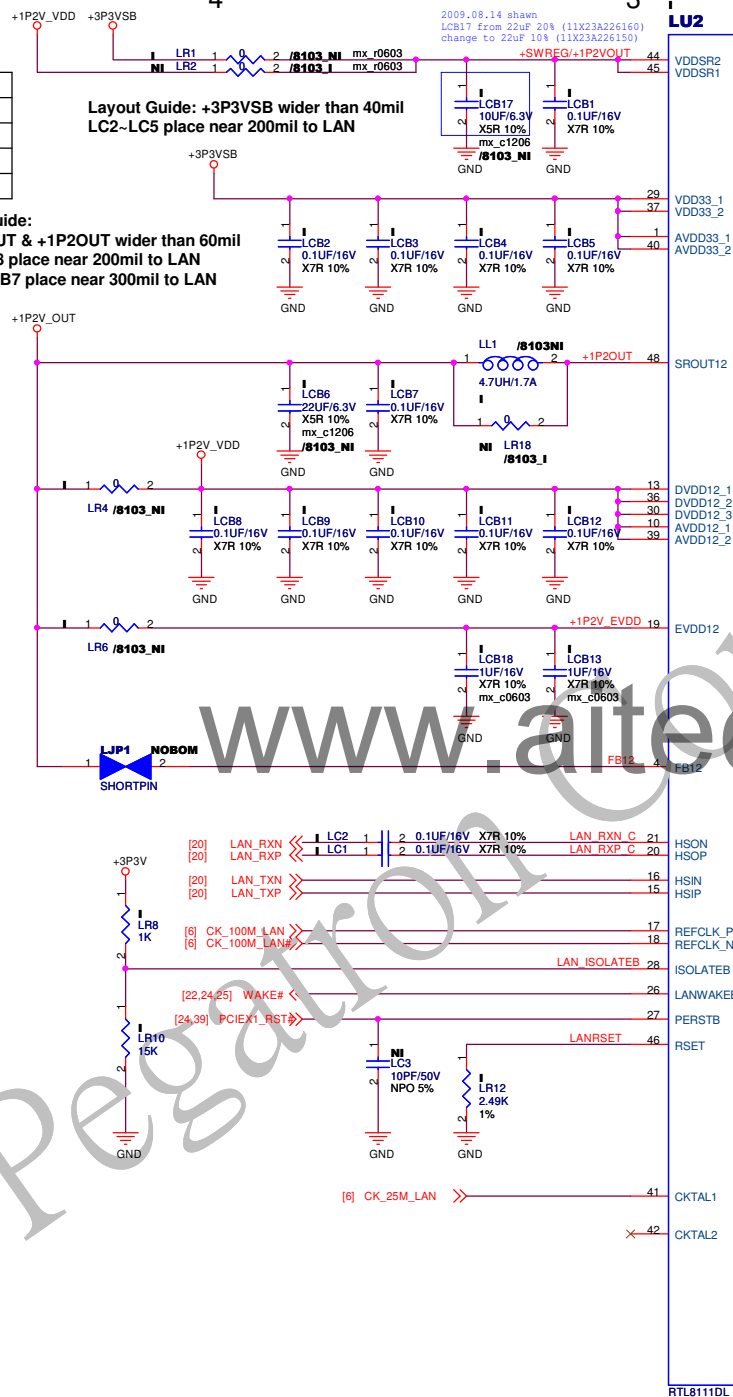
PIN	PIN NAME	I/O	Function
48	REG_OUT	O	<i>Regulator output</i>
4	FB12	I	<i>Feedback pin</i>
43	ENSWREG	I	<i>3.3V : Enable ; 0V : disable</i>
44,45	VDDREG	P	<i>3.3V power pin</i>

PIN	PIN NAME	I/O	Function
48	REG_OUT	O	<i>Regulator output</i>
4	FB12	I	<i>Feedback pin</i>
43	ENSWREG	I	<i>3.3V : Enable ; 0V : disable</i>
44,45	VDDREG	P	<i>3.3V power pin</i>

+1P2V_OUT & +1P2OUT wider than 60mil
LL1&LR18 place near 200mil to LAN
LCB6&LCB7 place near 300mil to LAN

8103EL	Pin
DVDD3.3V	29,37
AVDD3.3V	1
DVDD1.2V	10,13,30,36
+1.2V_OUT	19,45,48

8111DL	Pin
DVDD3.3V	29,37
AVDD3.3V	1,40
DVDD1.2V	13,36
AVDD1.2V	10,30,39
EVDD1.2V	19
+1.0V_OUT	48



If using eFuse function,
NI LU2 directly

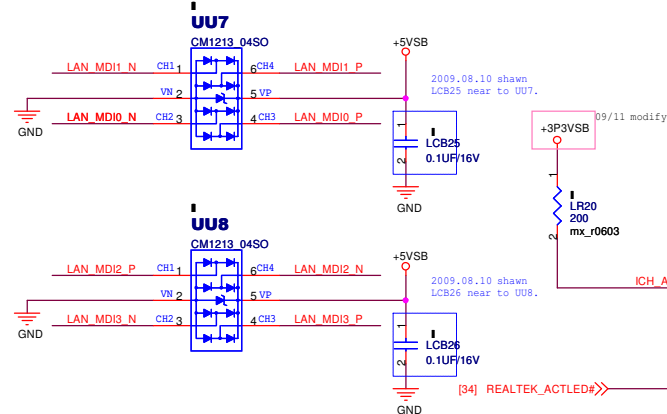
(LEDS1, LEDS0) = (1, 1) DEFAULT
(LEDS1, LEDS0) = (0, 1) ==> For this schematic

3.3V enable internal regulator
0V disable internal regulator

Symbol	Type	Pin No (64-pin)	Pin No (48-pin)	Description
LED0	O	57	38	LED0
LED1	O	56	35	LED1
LED2	O	55	34	LED2
LED3	O	54	33	LED3
				LED4
				LED5
				LED6

PEGATRON Title : AR8121 CONTROLLER

Pegatron Corp.		Engineer:	Tiepic Zhu	
Size A3	Project Name IPX41-D3			Rev 1.02
Date: Thursday, December 10, 2009		Sheet	34	of 54



LAN + Dual USB CONNECTOR

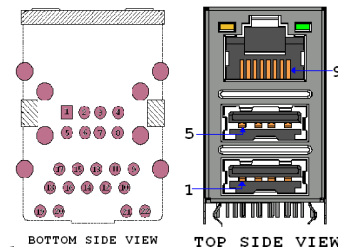
12XA05MYJG40

giga LAN connector

/Change to 12XA070YG040 for 10/100

J9

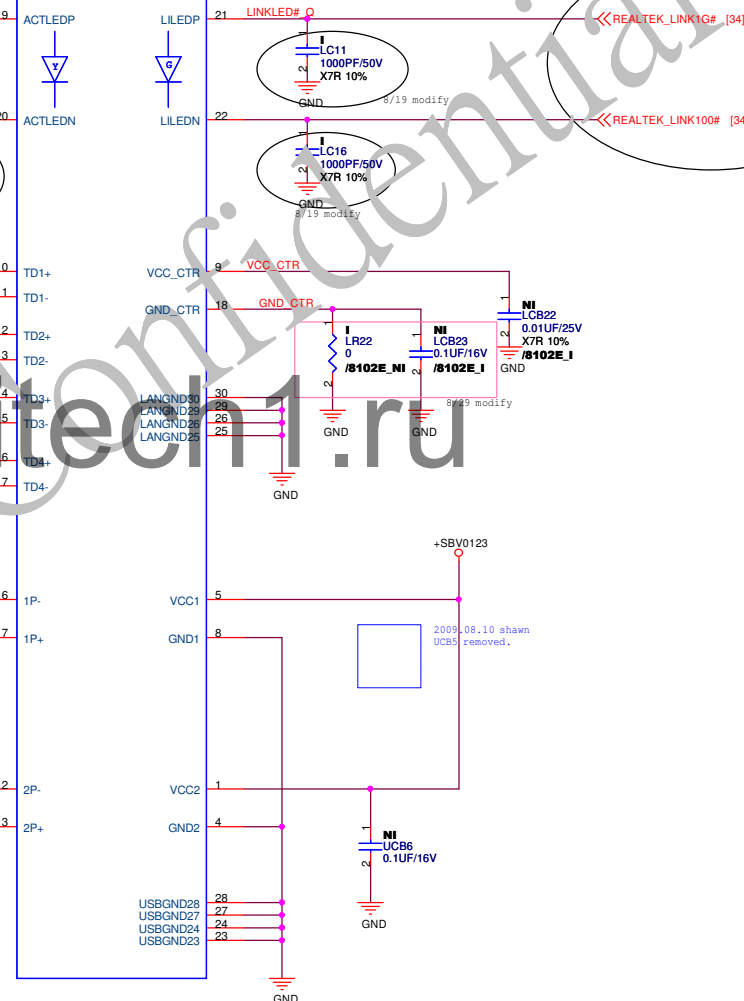
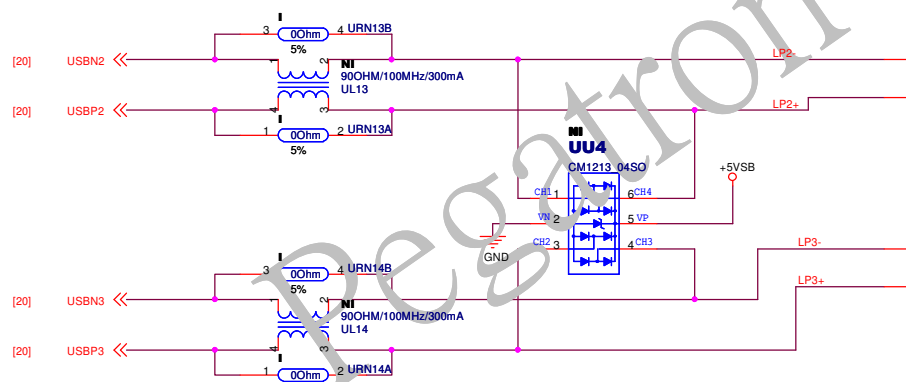
JACK USB/LAN GIGA



10/2 modify



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PEGATRON DT-MB RESTRICTED SECRET

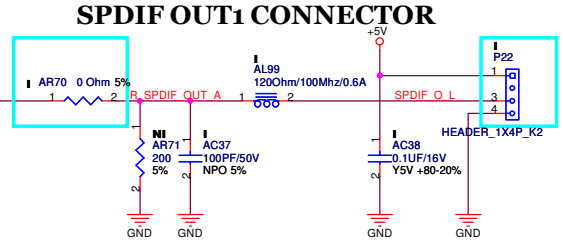
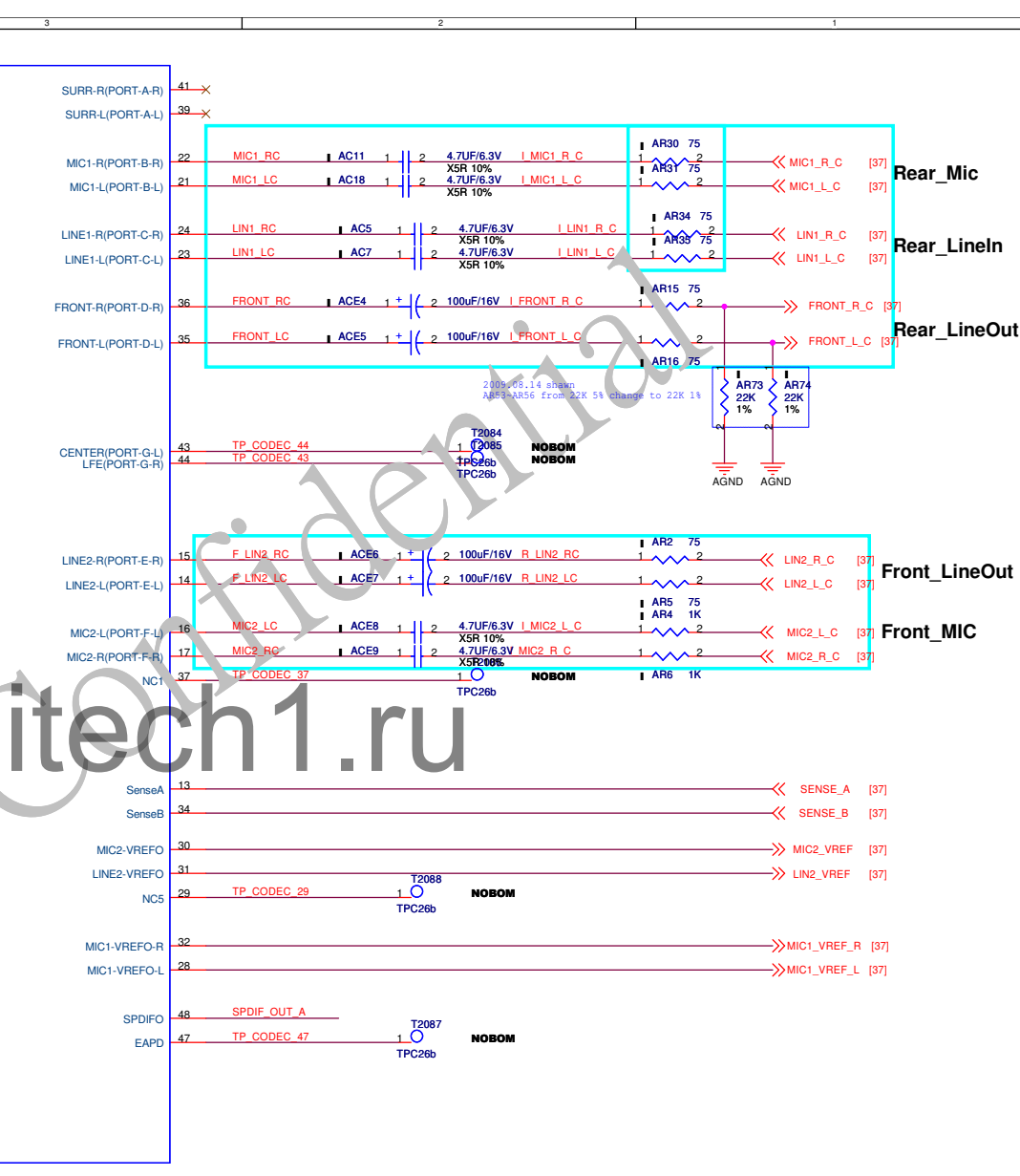
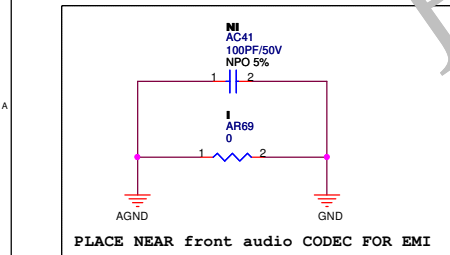
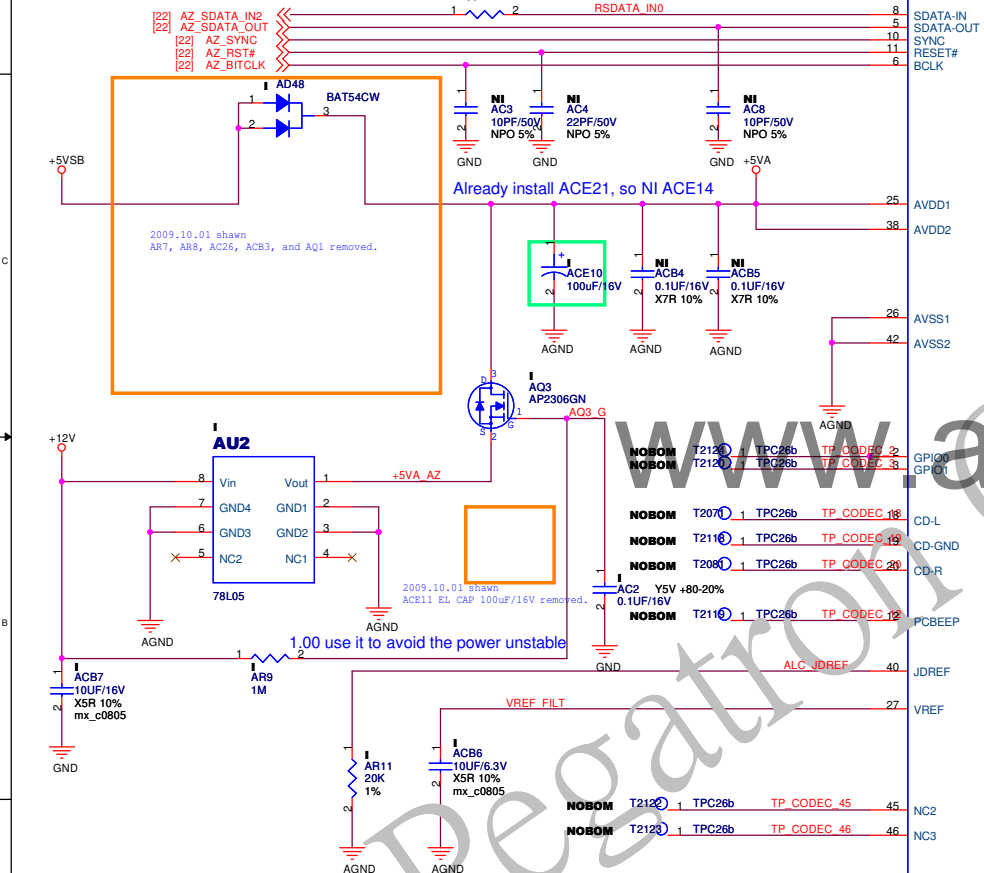
PEGATRON Title : RJ45+USB CONN.

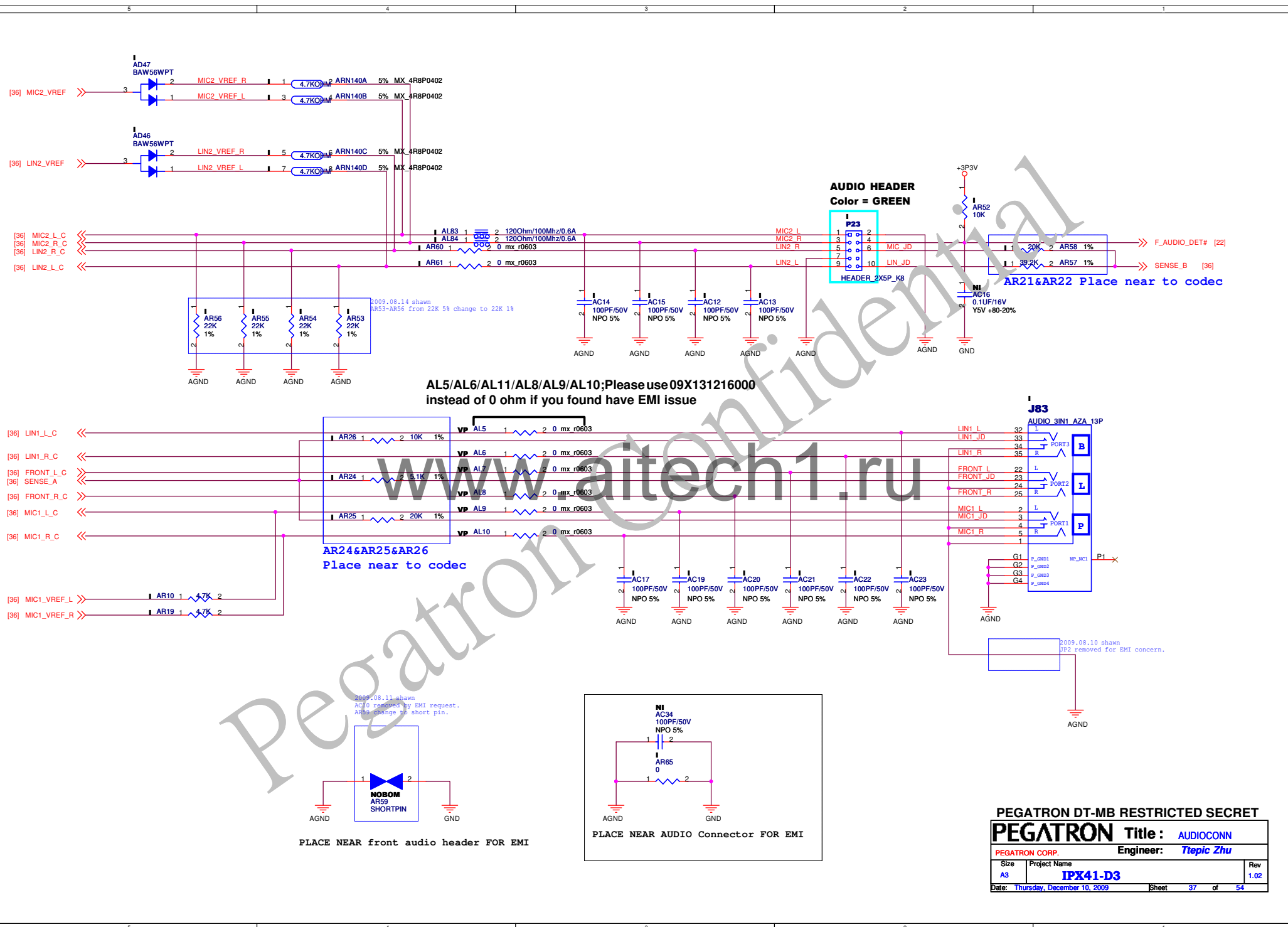
PEGATRON CORP. Engineer: Tjepic Zhu

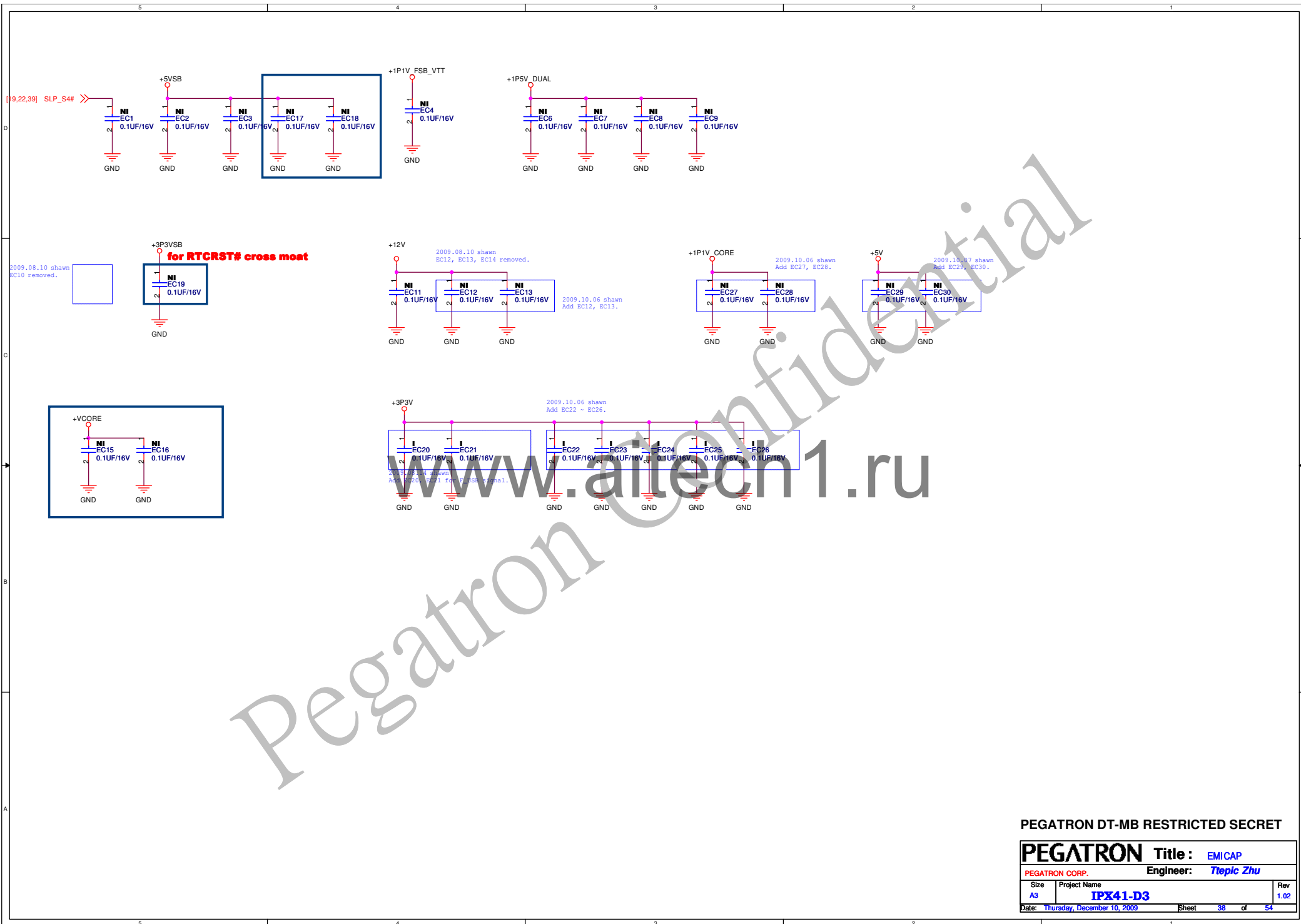
Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 35 of 54

Change to alc 662

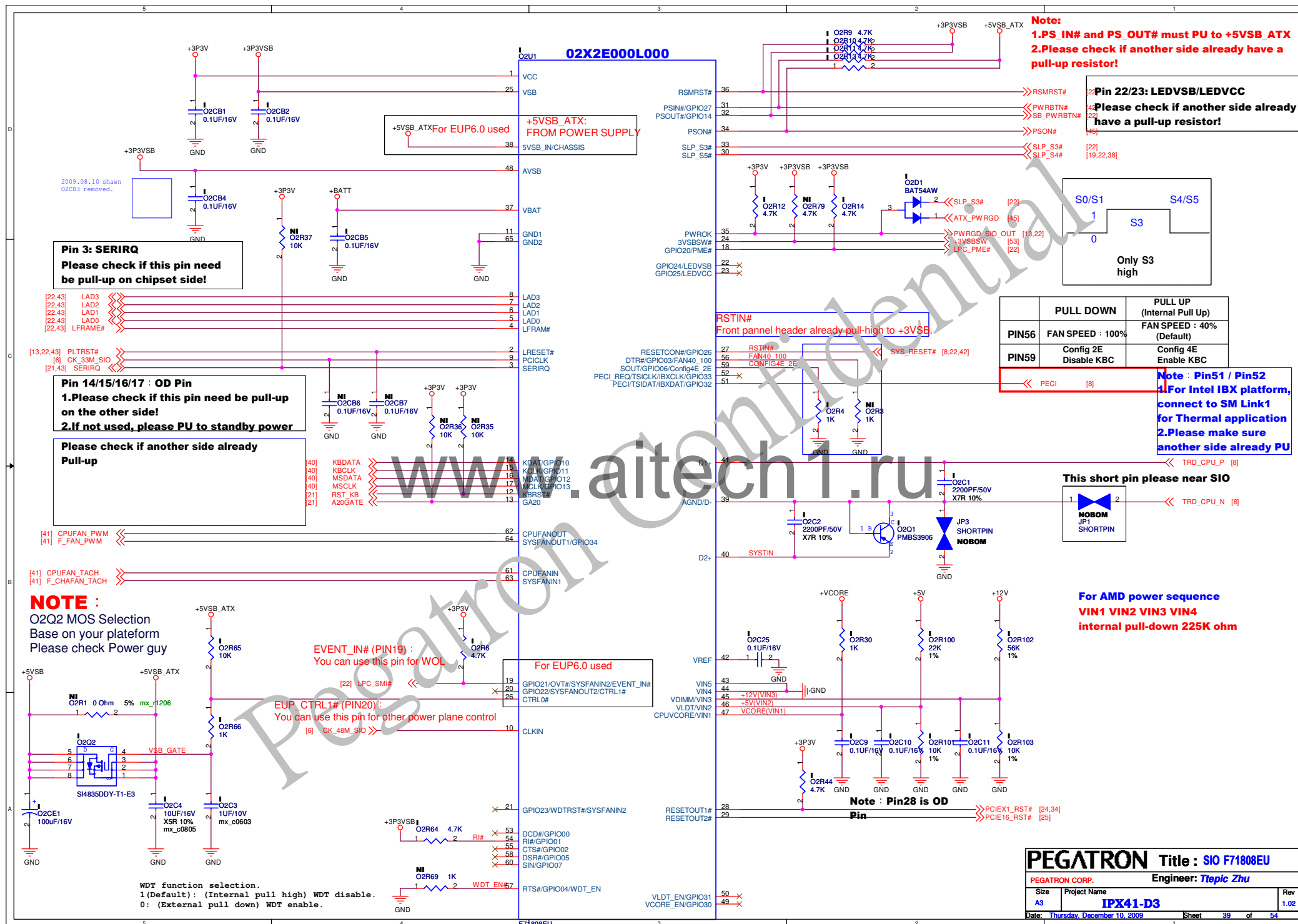




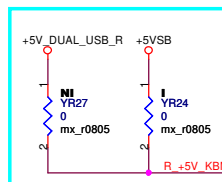


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title: EMICAP	
PEGATRON CORP.		Engineer: Tiepic Zhu	
Size A3	Project Name IPX41-D3	Rev 1.02	
Date: Thursday, December 10, 2009		Sheet 38 of 54	



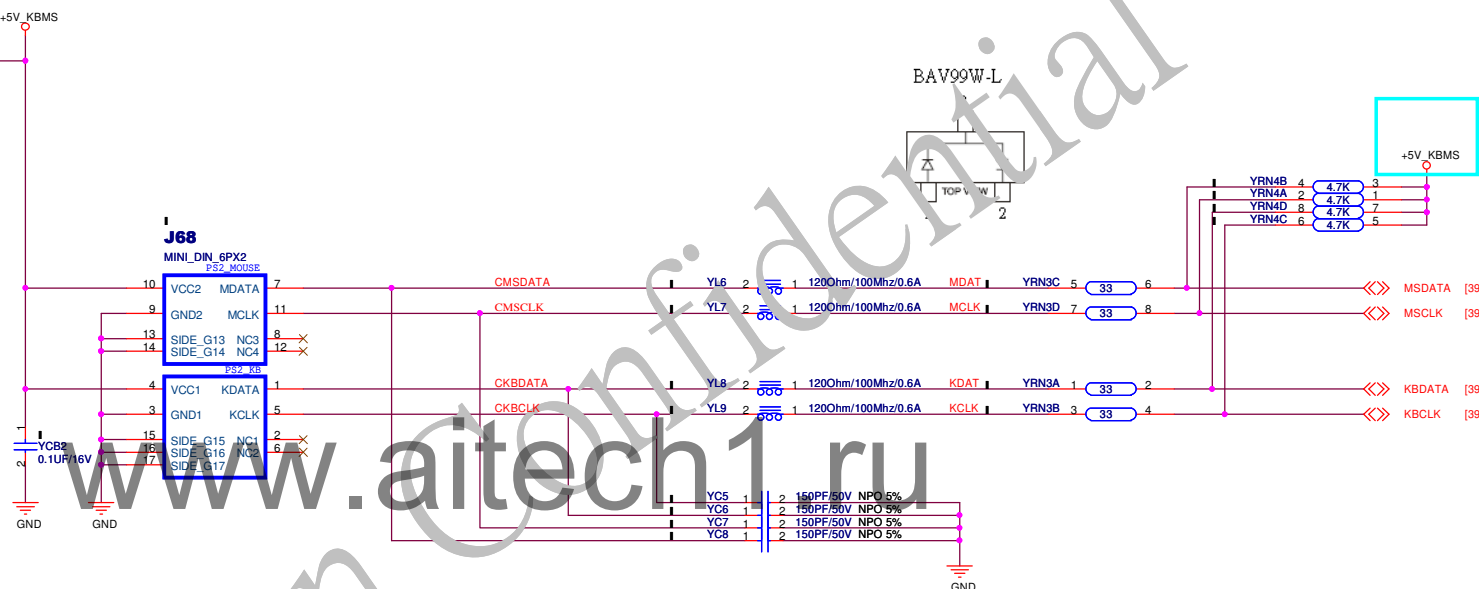
ADD FOR PS/2 WAKE ON IN S5



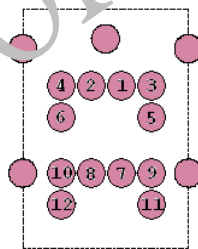
Note:

The +5V_DUAL_USB_B power trace width must have 40 mils or more

PS/2 KEYBOARD & MOUSE FOR CPC



TOP SIDE VIEW



BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

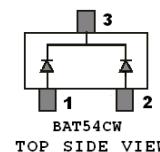
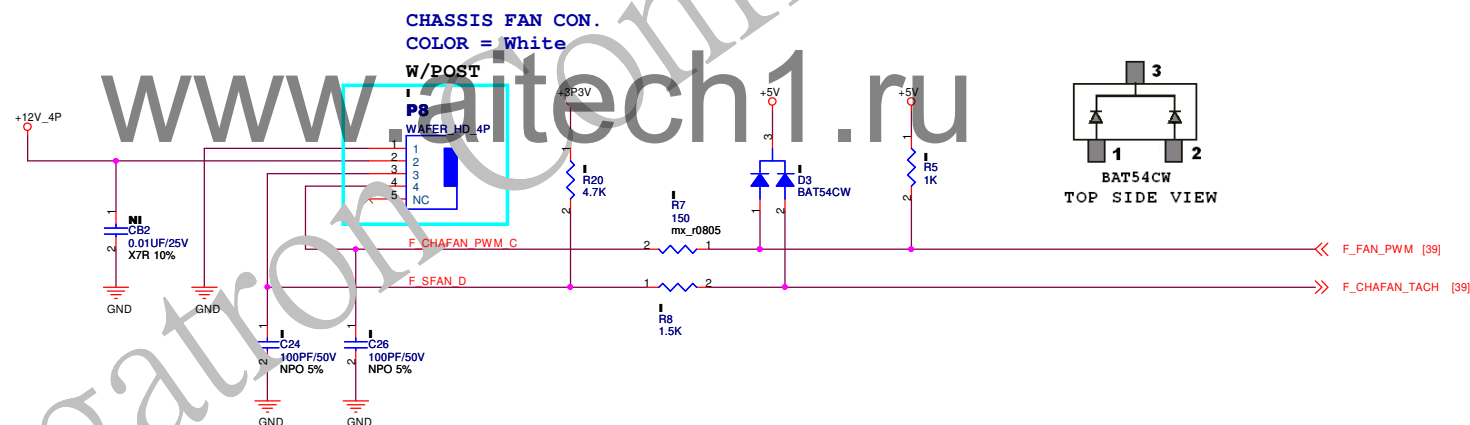
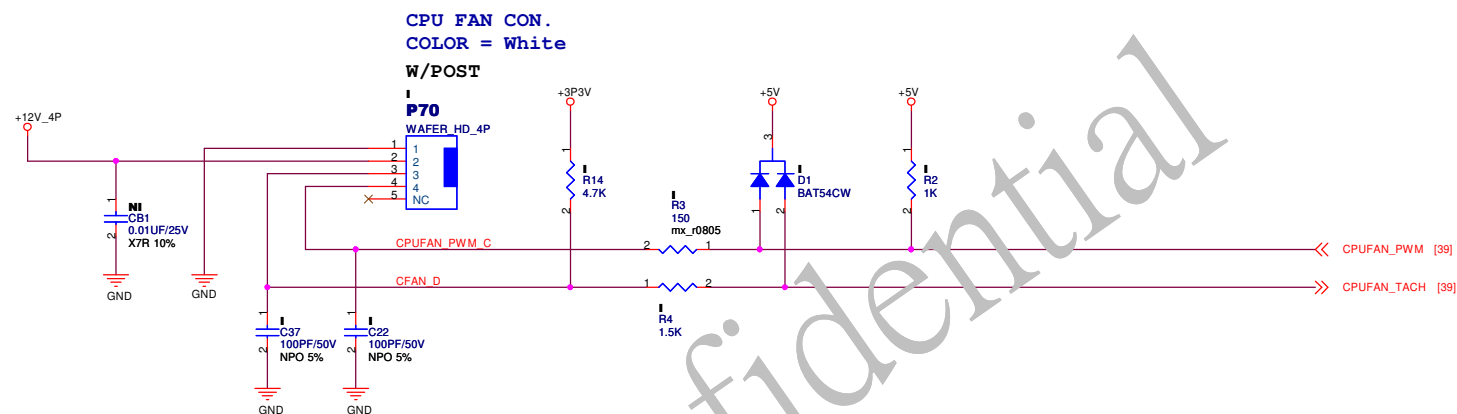
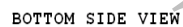
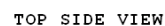
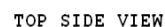
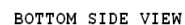
PEGATRON Title : KB & MS FOR CPC

PEGATRON CORP. Engineer: *Tiepic Zhu*

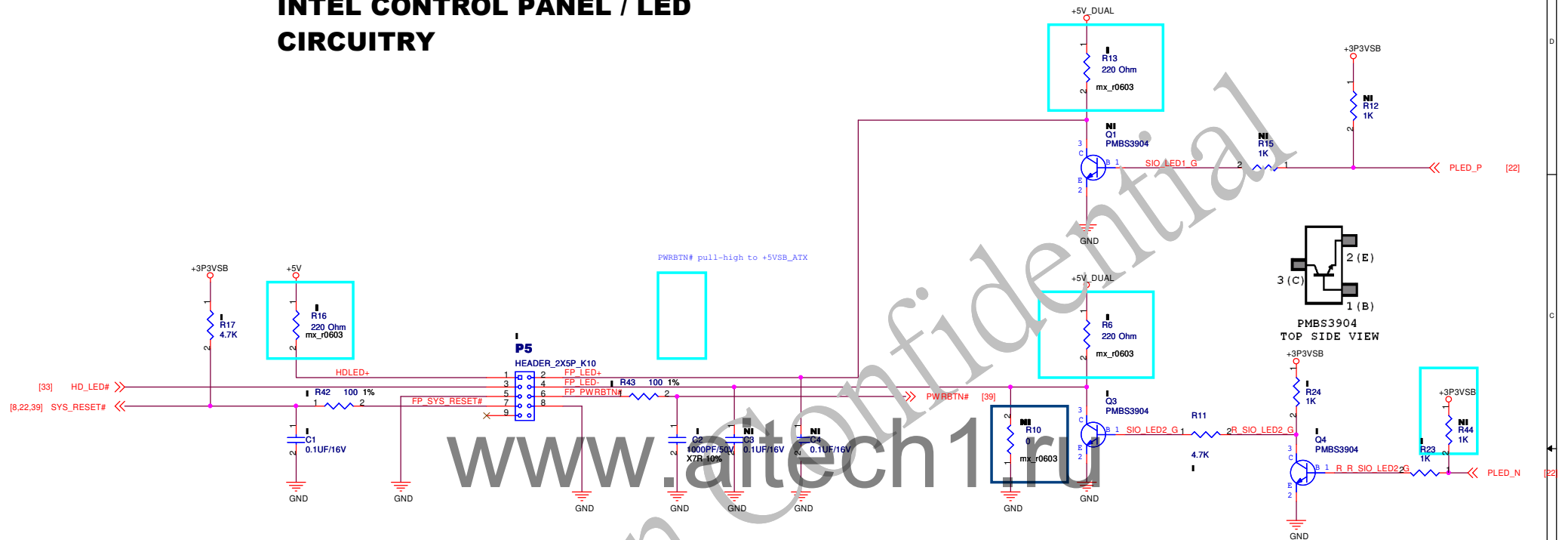
Size	Project Name	Res
100	IBM1 PC	

A3	IPX41-D3	1.0
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Date: Thursday, December 10, 2009 Sheet 40 of 54



INTEL CONTROL PANEL / LED CIRCUITRY



FRONT POWER LED COLOR SUPPORT	R10	Q2	R6	R11
SINGLE	I	NI	NI	NI
COLOR DUAL	NI	I	I	I
COLOR				

Pin header connection diagram for the P12 module. The diagram shows connections for +3P3V, +3P3VSB, and GND to various pins of the 20-pin header. Signal lines include CK_33M_TPM, LFRAME#, LPC_RST#_TPM, LAD3, LAD0, LR25, LPCPD#, LAD2, LAD1, SERIRQ, and CLKRUN#. A note indicates that VCI6 was removed on 2009.08.13.

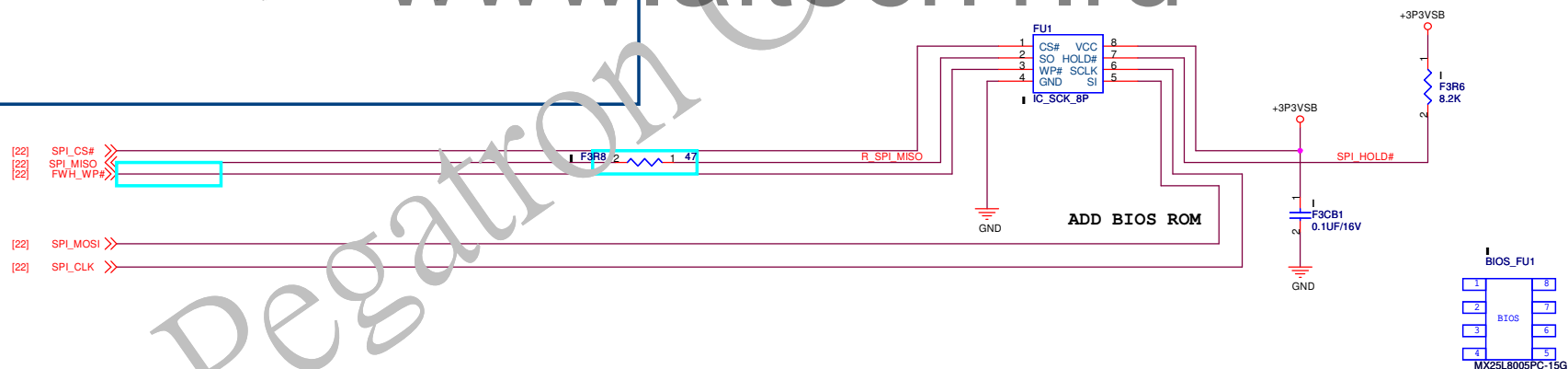
[illegible]

Diagram showing the pinout for the NOBOM SP78 module. The module is connected to a 6-pin header. The connections are as follows:

- Pin 1: MFG_NET
- Pin 2: GND
- Pin 3: GND
- Pin 4: GND
- Pin 5: GND
- Pin 6: GND

The module is labeled NOBOM SP78 and PEGATRON_MFG.

SPI BIOS ROM - 8Mbit



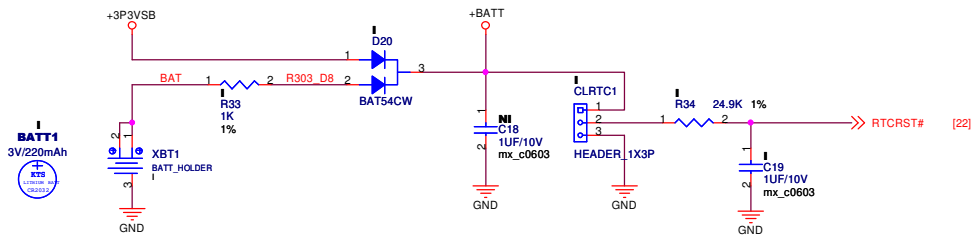
External RTC Circuitry

CLEAR CMOS

CLRTC1:12

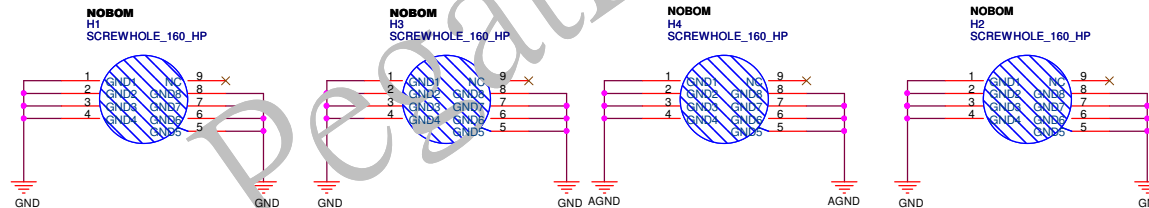
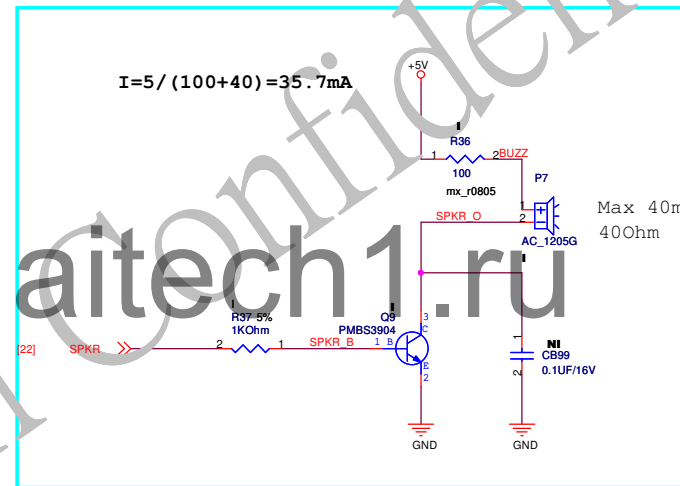
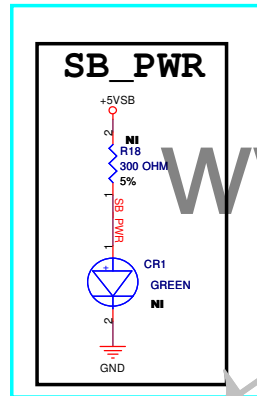


CMOS RTC	
1-2	Default
2-3	CLEAR



Battery Socket

SPEAKER



ONLY FOR SCREW
HOLE

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title: RTC / CMOS / SPKR

PEGATRON CORP. Engineer: Tepic Zhu

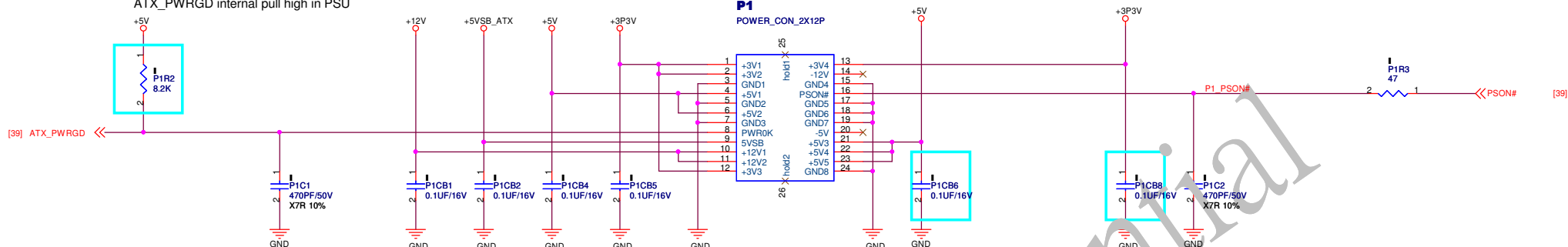
Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 44 of 54

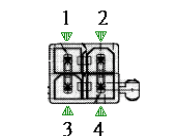
ATX POWER_24P SUPPLY CONNECTOR

NOTE:

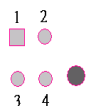
ATX_PWRGD internal pull high in PSU



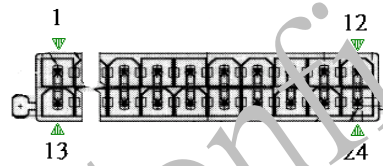
All of the Caps Around the ATX Power Connector



TOP SIDE VIEW



BOTTOM SIDE VIEW

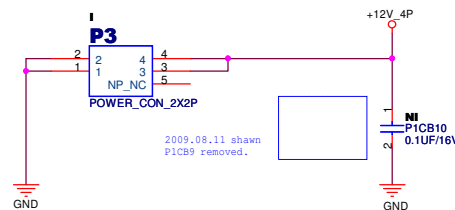


TOP SIDE VIEW

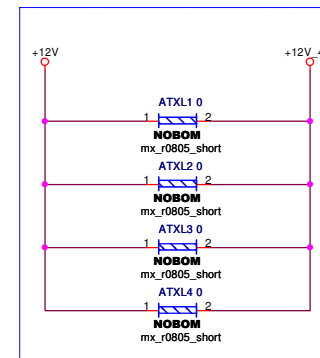


BOTTOM SIDE VIEW

VRM POWER_4P SUPPLY CONNECTOR



2009.08.04 shawn
→ Remove E70, E71 header and jumper
→ Add ATXL1 - 4 0805 short pin for keep the +12V trace width.



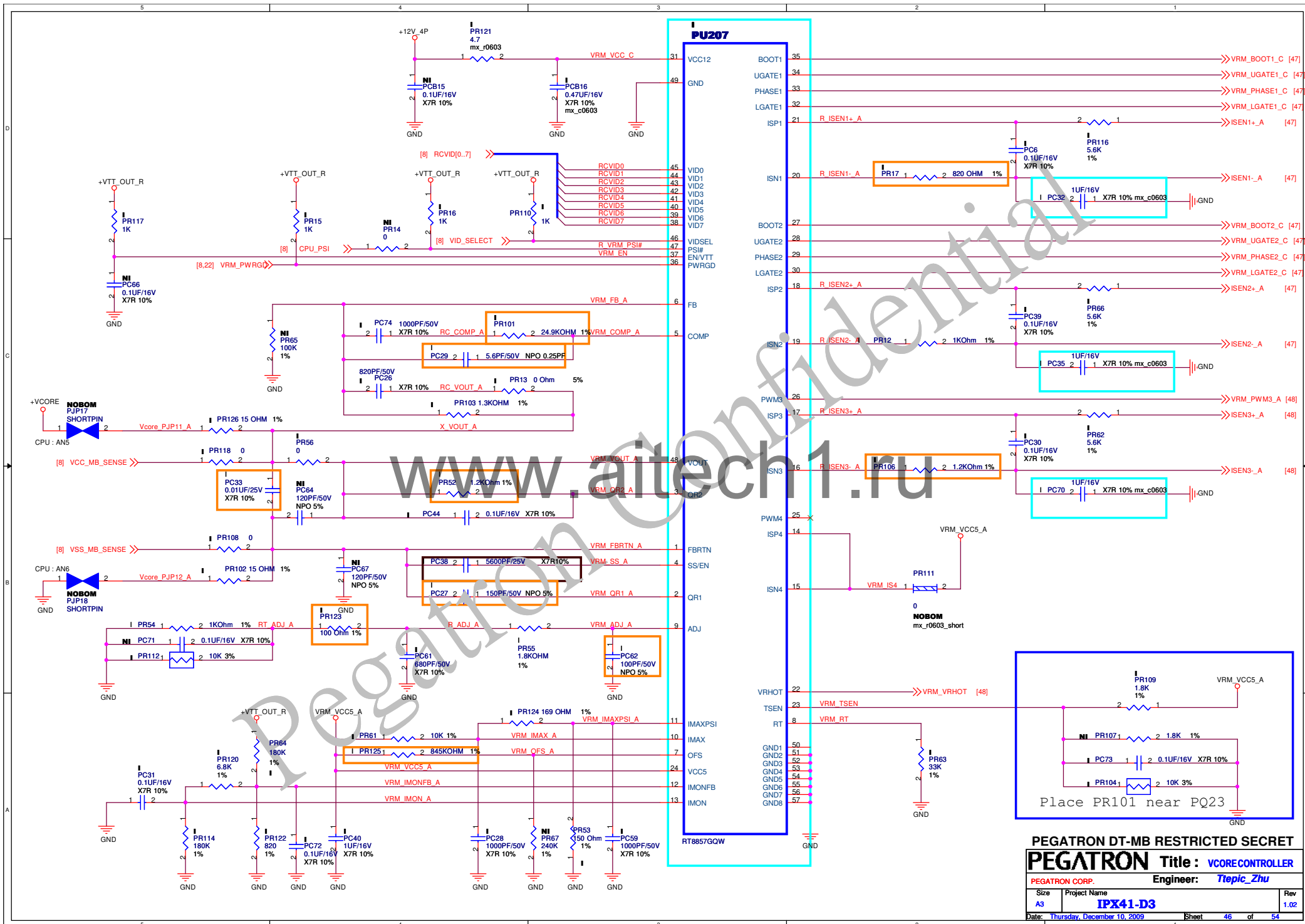
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title: **ATX POWER**

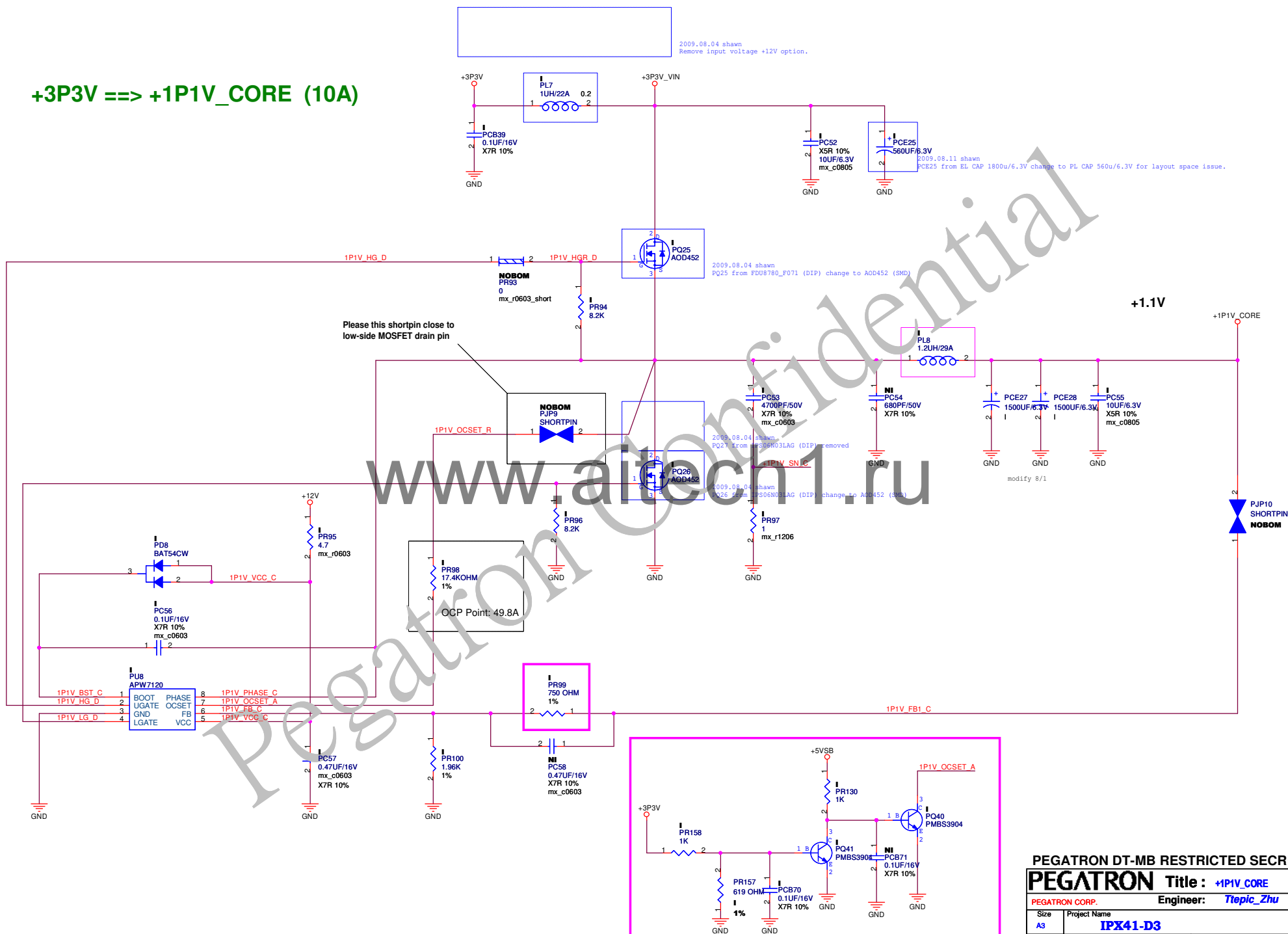
PEGATRON CORP. Engineer: **Tiepic Zhu**

Size A3 Project Name **IPX41-D3** Rev

Date: Thursday, December 10, 2009 Sheet 45 of 54



+3P3V ==> +1P1V_CORE (10A)



PEGATRON DT-MB RESTRICTED SECRET

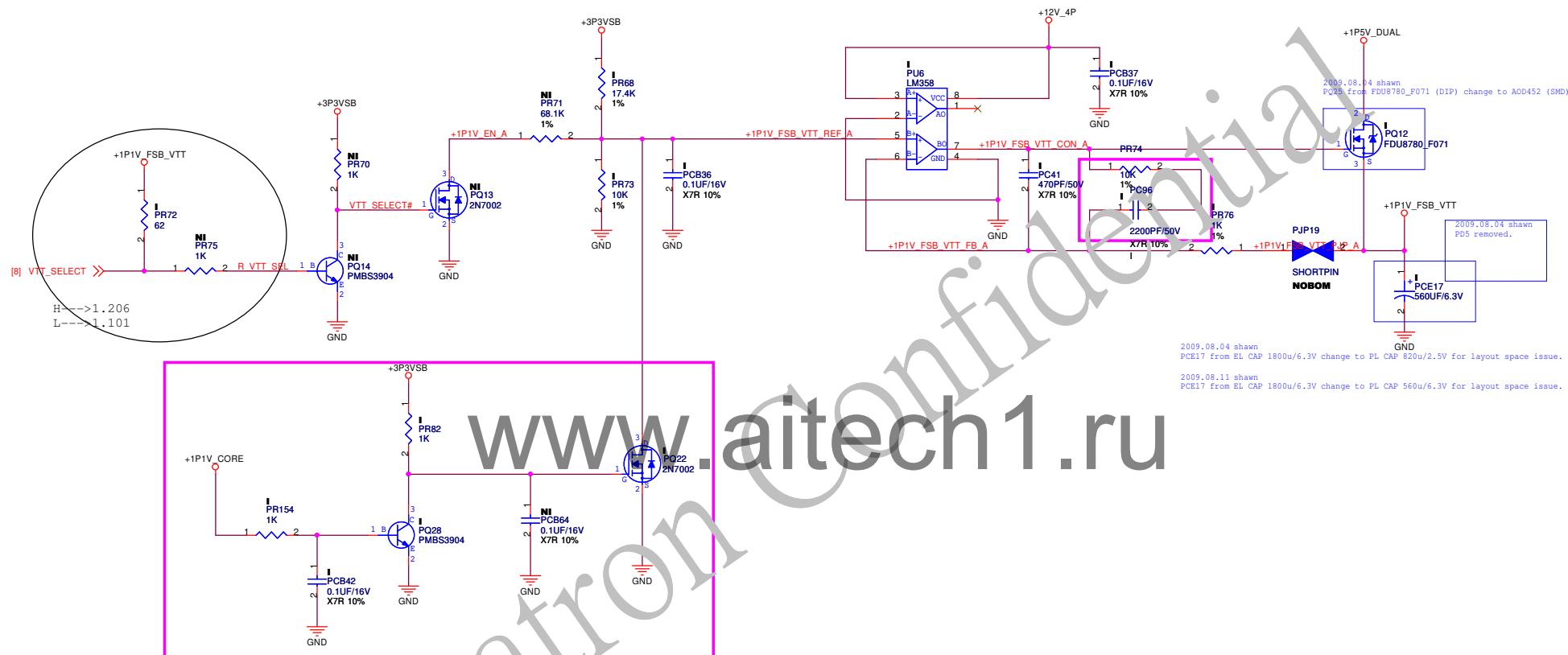
PEGATRON Title: +1P1V_CORE

PEGATRON CORP. Engineer: Ttepic_Zhu

Size A3	Project Name IPX41-D3	Rev 1.02
-------------------	---------------------------------	--------------------

Date: Thursday, December 10, 2009 Sheet 49 of 54

+1P5V_DUAL ==> +1P1V_FSB_VTT (1.5A)



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P1V_FSB_VTT_LDO

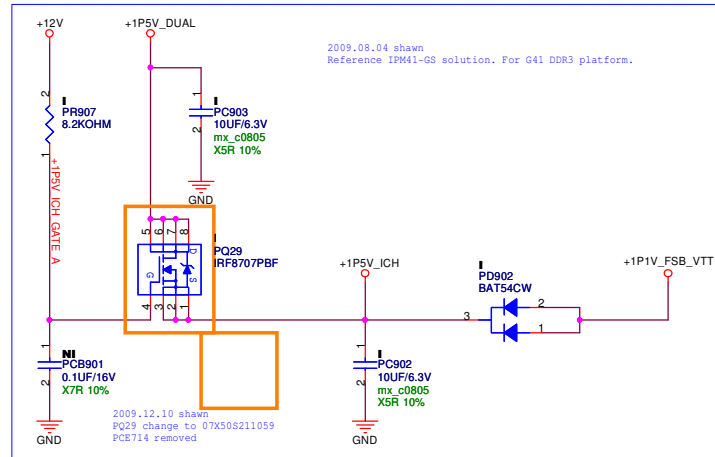
PEGATRON CORP. Engineer: Tetric_Zhu

Size Project Name IPX41-D3 Rev 1.02

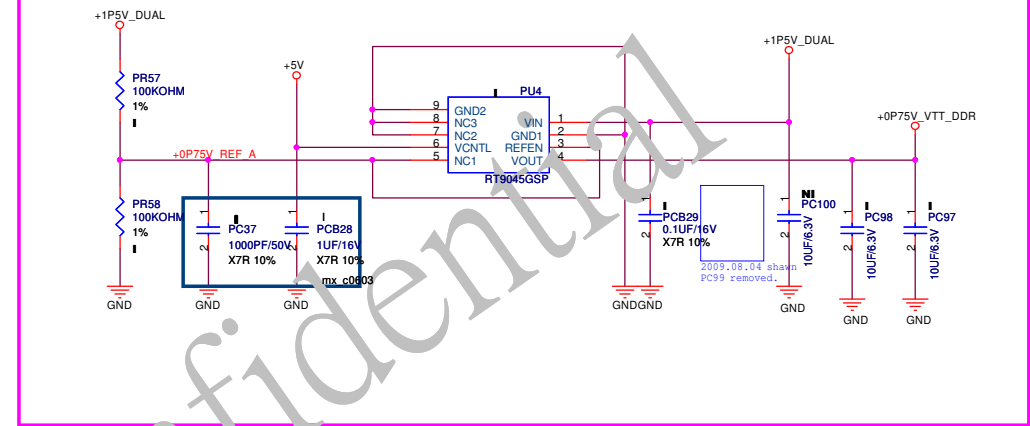
Date: Thursday, December 10, 2009 Sheet 50 of 54

+1P5V_DUAL ==> +1P5V_ICH (2A)

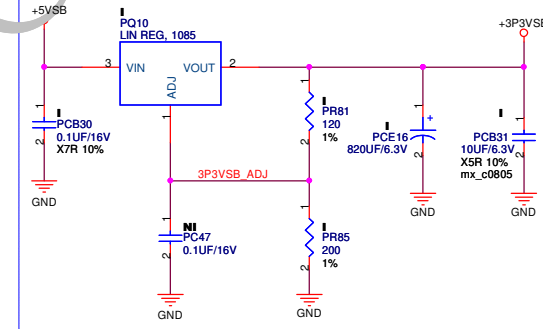
+1P5V_ICH (2A) For G41 DDR3 Platform



+1P5V_DUAL ==> +0P75V_VTT_DDR (2A)



+5VSB ==> +3P3VSB (1.5A)



2009.08.04 shawn
 -> Removed switch regulator solution.
 -> Add Linear regulator solution.

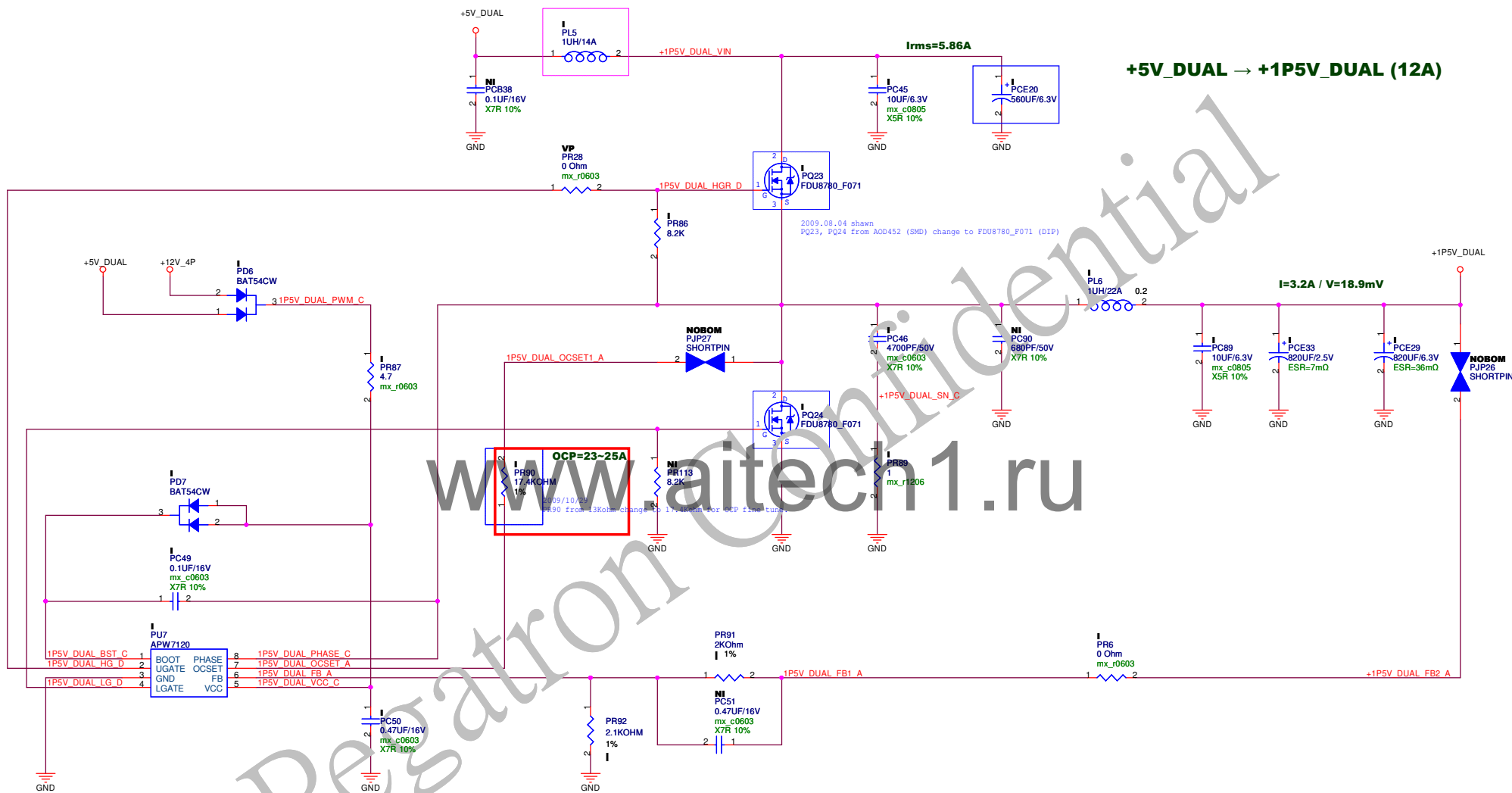
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +0P9V_VTT_DDR LDO

PEGATRON CORP. Engineer: Tetric_Zhu

Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 51 of 54



PEGATRON DT-MB RESTRICTED SECRET

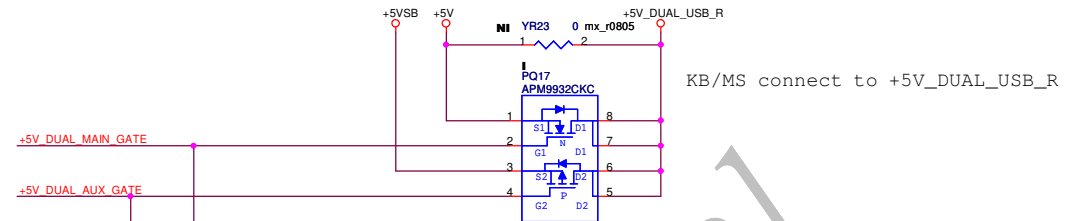
PEGATRON Title : +1P5V_DUAL_SW

PEGATRON CORP. Engineer: Teping_Zhu

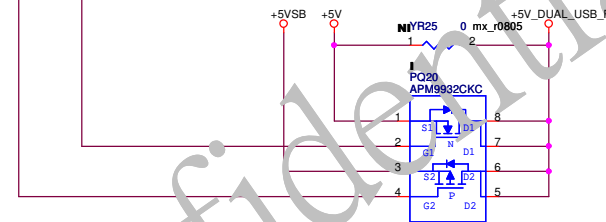
Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 52 of 54

+5V_DUAL_USB_R.....3A



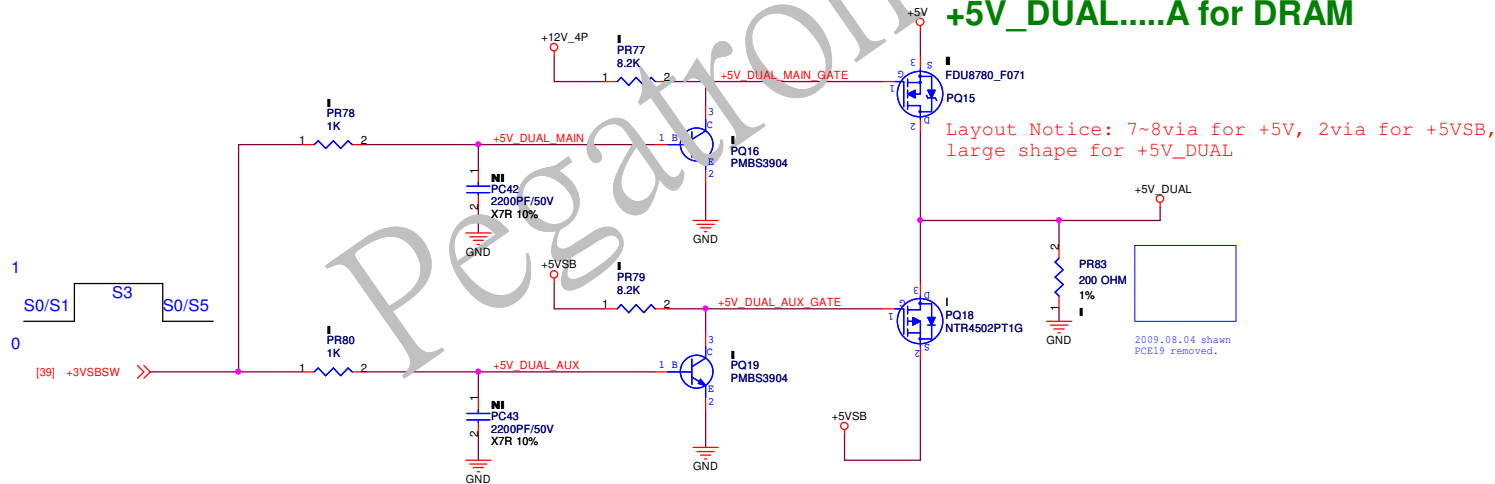
+5V_DUAL_USB_F.....3A



Layout Notice: 3~4via for +5V, 2via for +5VSB,
large shape for +5V_DUAL

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+5V_DUAL.....A for DRAM



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +IP1V_FSB_VTT_LDO

PEGATRON CORP. Engineer: Ttepic_Zhu

Size A3 Project Name IPX41-D3 Rev 1.02

Date: Thursday, December 10, 2009 Sheet 53 of 54

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PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : +3P3V_PCIE&+3P3V_LAN	
PEGATRON COMPUTER INC		Engineer: <u>Hemine_He</u>	
Size	Project Name		Rev
A3	IPX41-D3		1.02
Date: Thursday, December 10, 2009		Sheet	54 of 54